K3_DEB1_P1_LP5315B

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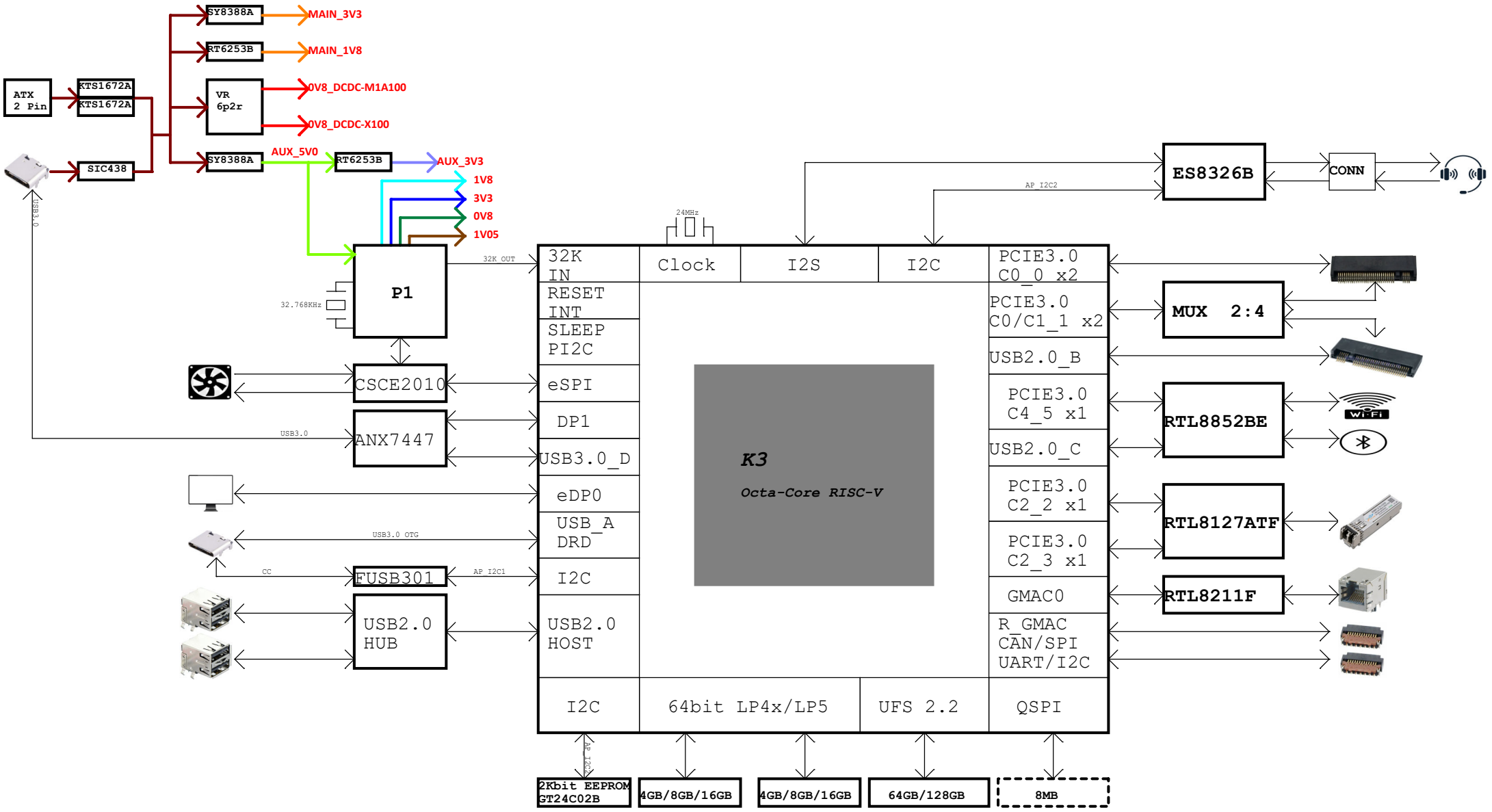
Block Diagram



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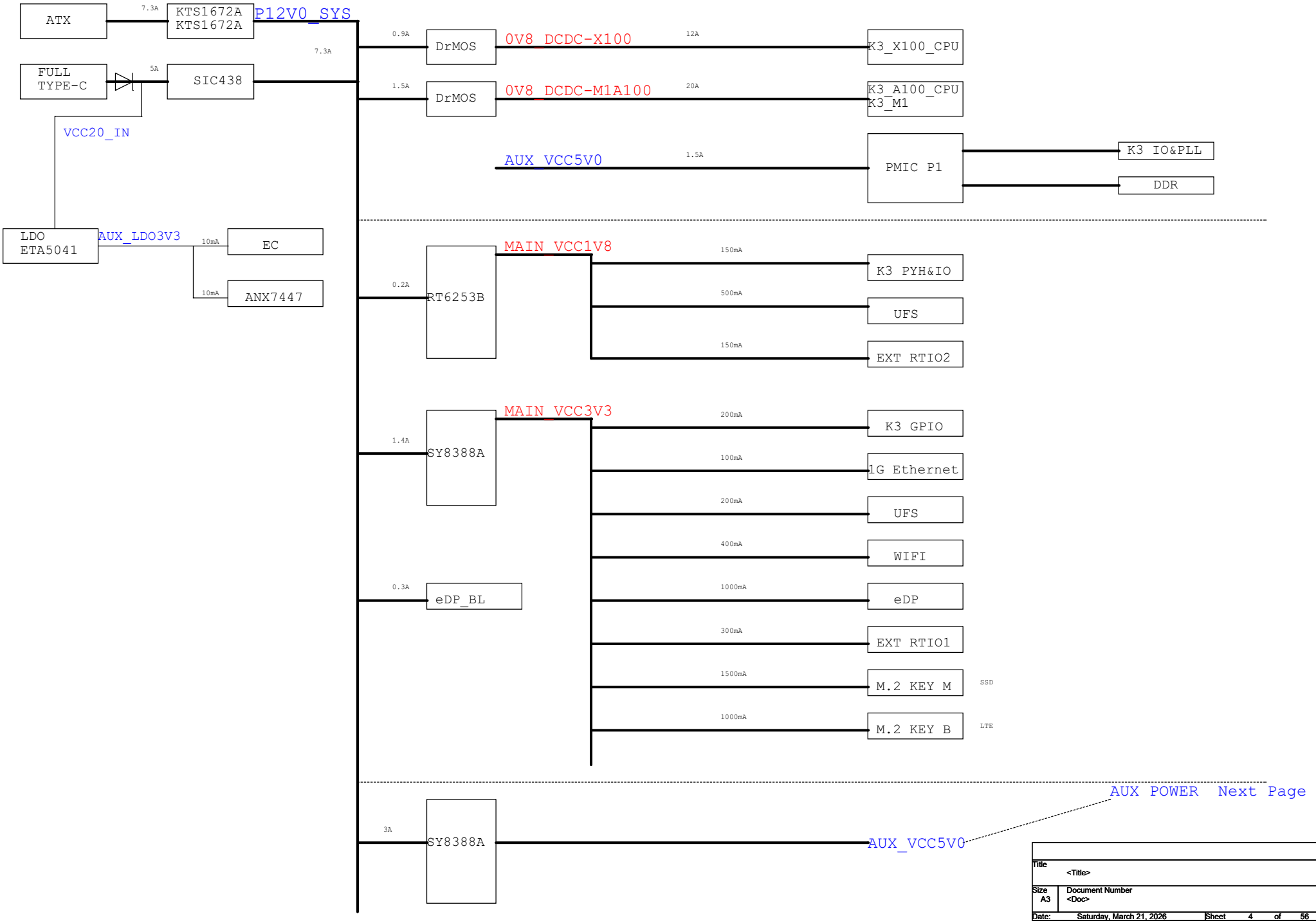
Power Tree



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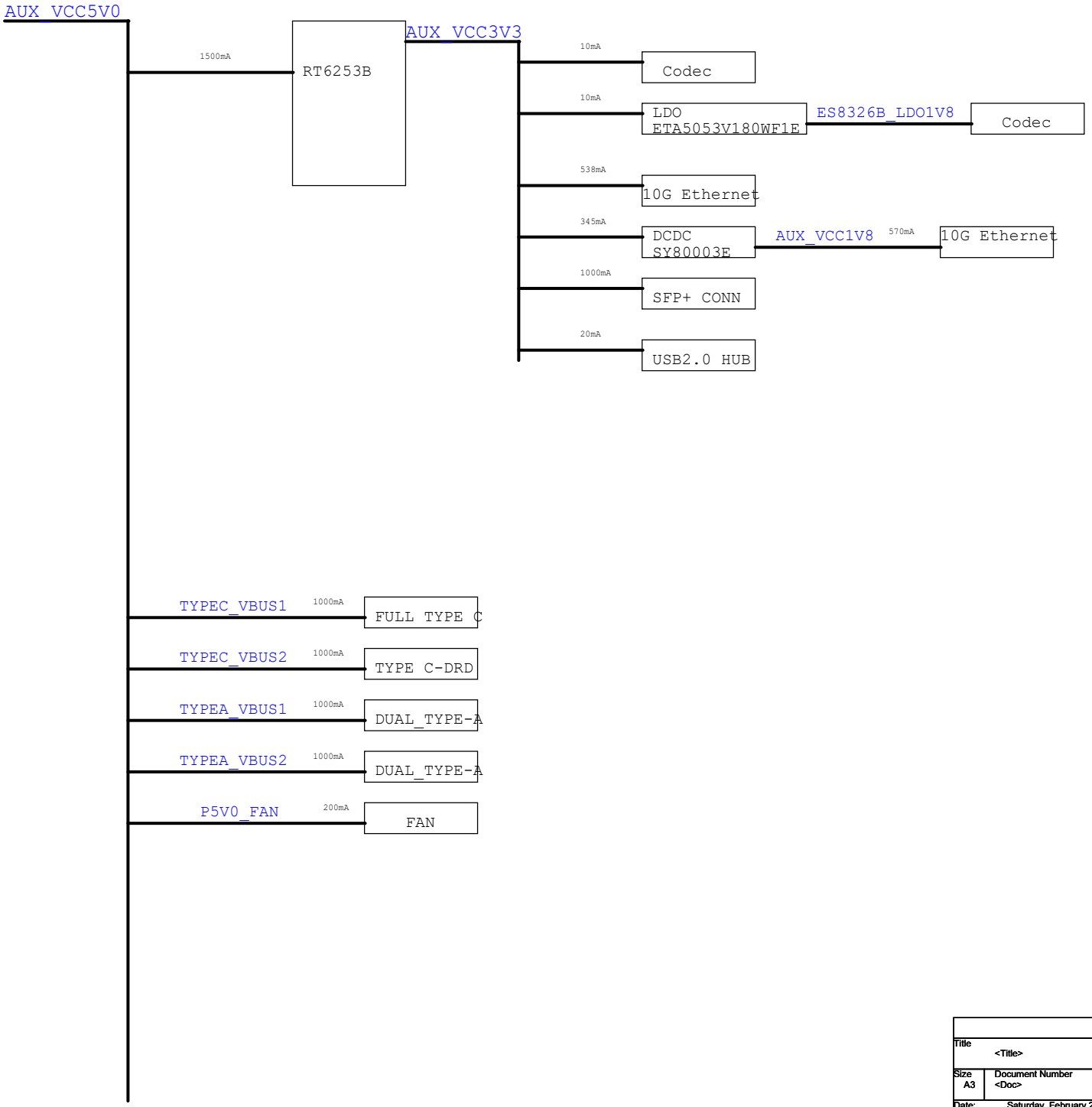
Power Tree



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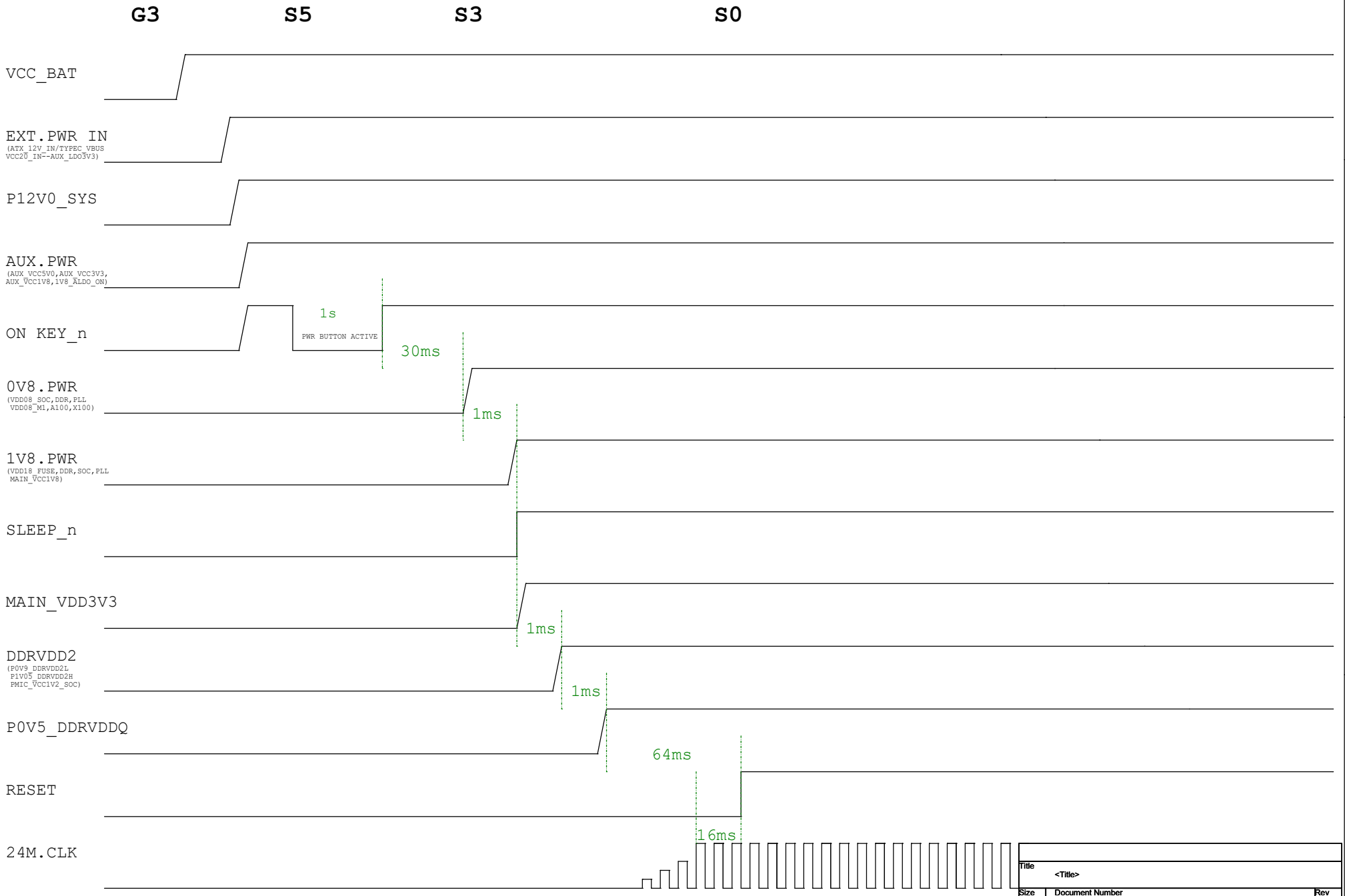
Power Sequence



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CLK MAP

updating...

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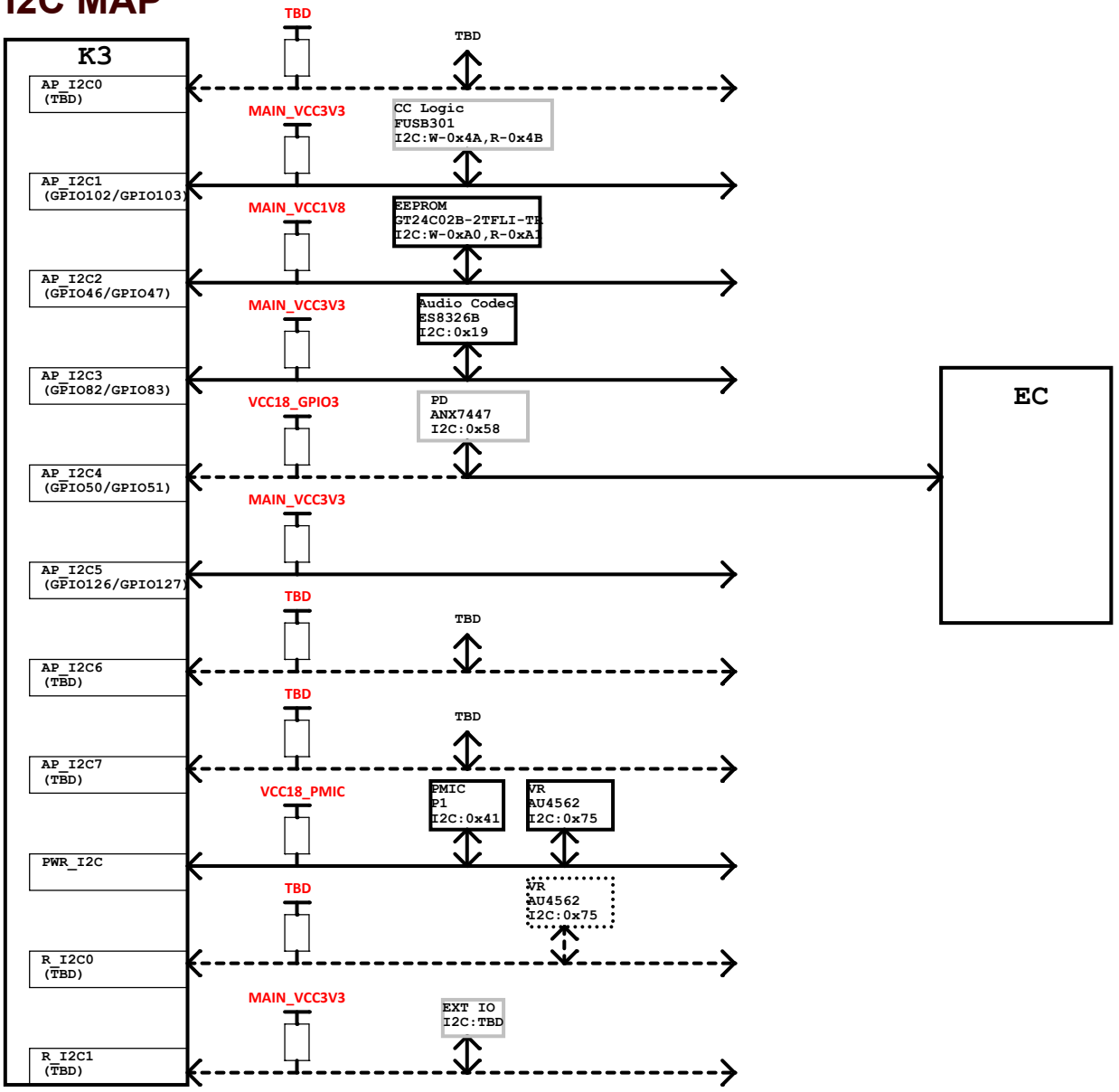
I2C MAP



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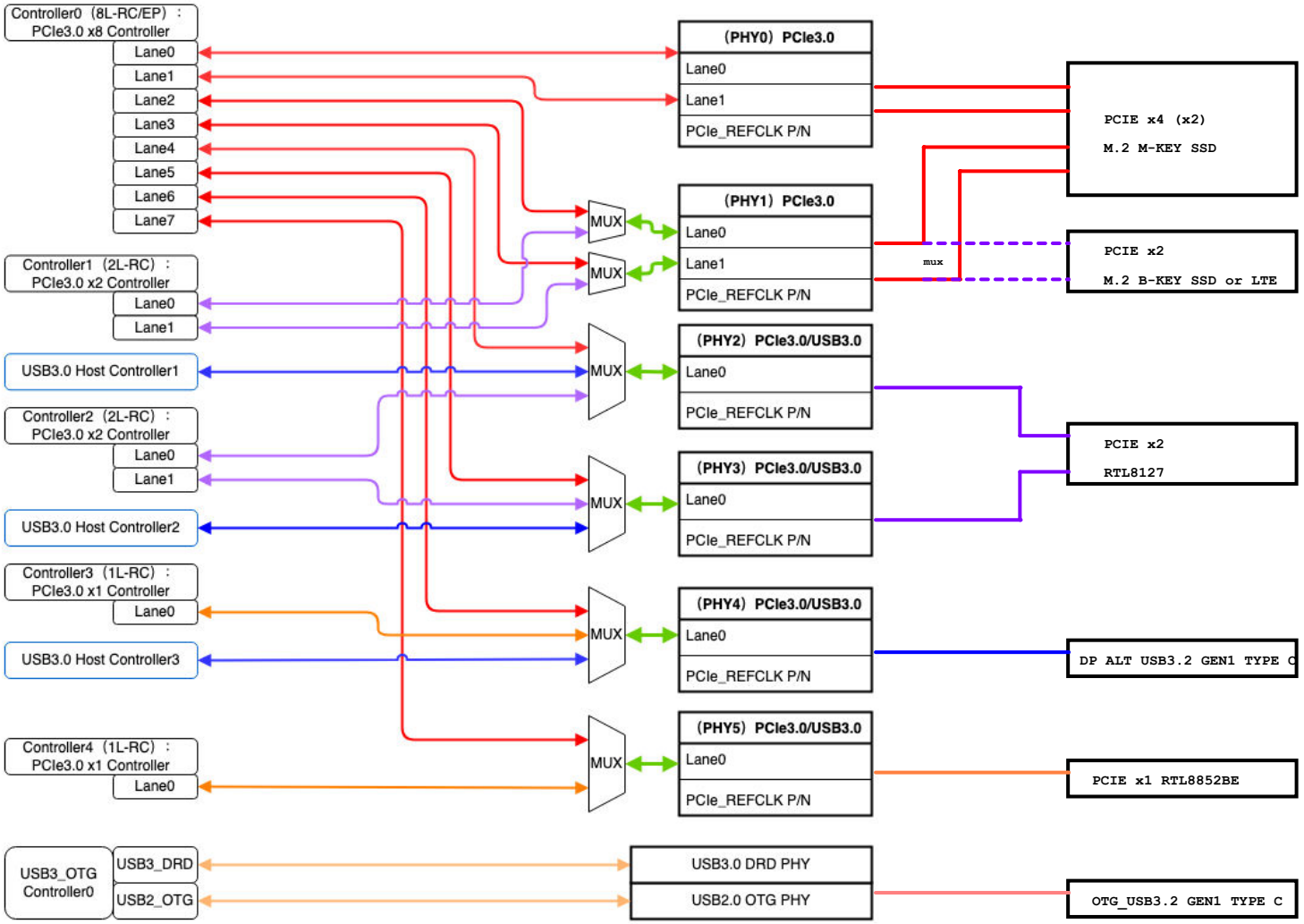
PCIE/USB MAP

M-KEY	B-KEY
M-KEY SSD x4	LTE or nothing
M-KEY SSD x2	B+M KEY SSD x2



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GPIO ASSIGNMENT

EC		
H34	GPIO[3]_42	EC_CPU_ALLPG
J34	GPIO[3]_43	EC_CPU_INT_N
AR34	GPIO[4]_80	SOC_EC_RST
AV34	GPIO[4]_82	CPU_EC_SWDIO
AW34	GPIO[4]_83	CPU_EC_SWCLK
AW36	GPIO[4]_91	ESPI0_D0
AY36	GPIO[4]_92	ESPI0_D1
AW37	GPIO[4]_93	ESPI0_D2
AY37	GPIO[4]_94	ESPI0_D3
AW38	GPIO[4]_95	ESPI0_CS
AV39	GPIO[4]_96	ESPI0_CLK
AW39	GPIO[4]_97	ESPI0_RESETN
AV40	GPIO[4]_98	ESPI0_ALRTN

CODEC		
C38	GPIO[2]_36	I2C3_SCL_3V3
D38	GPIO[2]_37	I2C3_SDA_3V3
AU26	GPIO[5]_111	BT_PCM_CLK_3V3
AW26	GPIO[5]_112	BT_PCM_SYNC_3V3
AY26	GPIO[5]_113	BT_PCM_OUT_3V3
AP25	GPIO[5]_114	BT_PCM_IN_3V3
AW24	GPIO[5]_122	CPU-I2S1_SCLK
AY24	GPIO[5]_123	CPU-I2S1_LRCK
AT23	GPIO[5]_124	CPU-I2S1_OUT
AU23	GPIO[5]_125	CPU-I2S1_IN
AV23	GPIO[5]_126	CPU-I2S1_SYSCLK
AY23	GPIO[5]_127	CODEC_IRQ_3V3

GMAC		
AY32	GPIO[1]_00	GMAC0_RXDV
AW32	GPIO[1]_01	GMAC0_RXD0
AV32	GPIO[1]_02	GMAC0_RXD1
AU32	GPIO[1]_03	GMAC0_RXCLK
AR32	GPIO[1]_04	GMAC0_RXD2
AP32	GPIO[1]_05	GMAC0_RXD3
AP31	GPIO[1]_06	GMAC0_TXD0
AR31	GPIO[1]_07	GMAC0_TXD1
AT31	GPIO[1]_08	GMAC0_TXCLK
AU31	GPIO[1]_09	GMAC0_TXD2
AW31	GPIO[1]_10	GMAC0_TXD3
AY31	GPIO[1]_11	GMAC0_TXEN
AW30	GPIO[1]_12	GMAC0_MDC
AT30	GPIO[1]_13	GMAC0_MDIO
AW29	GPIO[1]_14	GMAC0_INT_N
AY29	GPIO[1]_15	GMAC0_RSTN_L
AP29	GPIO[1]_20	GMAC0_REF0_CLK_25M

MISC		
AT29	GPIO[1]_18	MODULE_TURN_ON_1V8
AR29	GPIO[1]_19	WWAN_RESET#_1V8
B35	GPIO[2]_26	BT_WAKE_HOST_3V3
B36	GPIO[2]_30	BT_EN_3V3
C37	GPIO[2]_35	WLAN_EN_3V3
D40	GPIO[2]_41	HOST_WAKE_BT_3V3
AY34	GPIO[4]_84	CPU_W_DISABLE#1
AY33	GPIO[4]_85	CC_INT_N
AT35	GPIO[4]_86	USB30_DRD_DIR
AU35	GPIO[4]_87	PWRA_MODE_G4
AW35	GPIO[4]_89	MUX_CPU_M2B2
AU28	GPIO[5]_101	SOC_EDP0_PWR-EN_3V3
AV28	GPIO[5]_102	CC_I2C1_SCL_3V3
AY28	GPIO[5]_103	CC_I2C1_SDA_3V3
AP27	GPIO[5]_106	SOC_EDP0_BL-PWM_3V3
AW25	GPIO[5]_118	SOC_EDP0_BL-EN_3V3

PCIE		
A35	GPIO[2]_25	PCIE2_PERSTN_3V3_CN
C35	GPIO[2]_27	PCIE2_CLKREQN_33_CN
AR33	GPIO[4]_76	PCIE4_PERSTN
AT33	GPIO[4]_77	PCIE4_WAKEN
AP35	GPIO[4]_78	PCIE4_CLKREQN
AP34	GPIO[4]_79	PCIE0_PERSTN
AT34	GPIO[4]_81	PCIE0_CLKREQN
AV35	GPIO[4]_88	PCIE1_PERSTN
AT36	GPIO[4]_90	PCIE1_CLKREQN

R.GMAC		
K34	GPIO[3]_44	R-GMAC3_CRS
L34	GPIO[3]_45	R-GMAC3_COL
J38	GPIO[3]_59	R-GMAC3_RXDV
L38	GPIO[3]_60	R-GMAC3_RXD0
M38	GPIO[3]_61	R-GMAC3_RXD1
N38	GPIO[3]_62	R-GMAC3_RXCLK
P38	GPIO[3]_63	R-GMAC3_RXD2
J39	GPIO[3]_64	R-GMAC3_RXD3
K39	GPIO[3]_65	R-GMAC3_TXD0
L39	GPIO[3]_66	R-GMAC3_TXD1
M39	GPIO[3]_67	R-GMAC3_TXCLK
P39	GPIO[3]_68	R-GMAC3_TXD2
H40	GPIO[3]_69	R-GMAC3_TXD3
J40	GPIO[3]_70	R-GMAC3_TXEN
K40	GPIO[3]_71	R-GMAC3_MDC
L40	GPIO[3]_72	R-GMAC3_MDIO
M40	GPIO[3]_73	R-GMAC3_INT_N
N40	GPIO[3]_74	R-GMAC3_REF0_CLK_25M
P40	GPIO[3]_75	R-GMAC3_RSTN_L

R.GPIO		
A34	GPIO[2]_21	UART5_TXD_3V3
B34	GPIO[2]_22	UART5_RXD_3V3
D35	GPIO[2]_28	R-PWM1_3V3
A36	GPIO[2]_29	R-PWM2_3V3
C36	GPIO[2]_31	UART10_TXD_3V3
A37	GPIO[2]_32	UART10_RXD_3V3
B38	GPIO[2]_33	UART10_CTS_3V3
A38	GPIO[2]_34	UART10_RTS_3V3
D39	GPIO[2]_39	R-I2C1_SCL_3V3
C40	GPIO[2]_40	R-I2C1_SDA_3V3
J35	GPIO[3]_48	CAN1_RXD_1V8
K35	GPIO[3]_49	CAN1_TXD_1V8
L37	GPIO[3]_57	R-CAN0_RXD_1V8
M36	GPIO[3]_58	R-CAN0_TXD_1V8
AR28	GPIO[5]_99	R-CAN2_TXD_3V3
AT28	GPIO[5]_100	R-CAN2_RXD_3V3
AY27	GPIO[5]_107	R-CAN4_TXD_3V3
AP26	GPIO[5]_108	R-CAN4_RXD_3V3
AR26	GPIO[5]_109	R-UART0_TXD_3V3
AT26	GPIO[5]_110	R-UART0_RXD_3V3
AR24	GPIO[5]_120	R-CAN3_TXD_3V3
AT24	GPIO[5]_121	R-CAN3_RXD_3V3

SPI		
H36	GPIO[3]_53	SPI0_MOSI_1V8
H38	GPIO[3]_54	SPI0_MISO_1V8
H37	GPIO[3]_55	SPI0_SCLK_1V8
J37	GPIO[3]_56	SPI0_CS_1V8

DP		
C34	GPIO[2]_23	SOC_EDP0_HPD_3V3
E34	GPIO[2]_24	DP1_HPD_3V3

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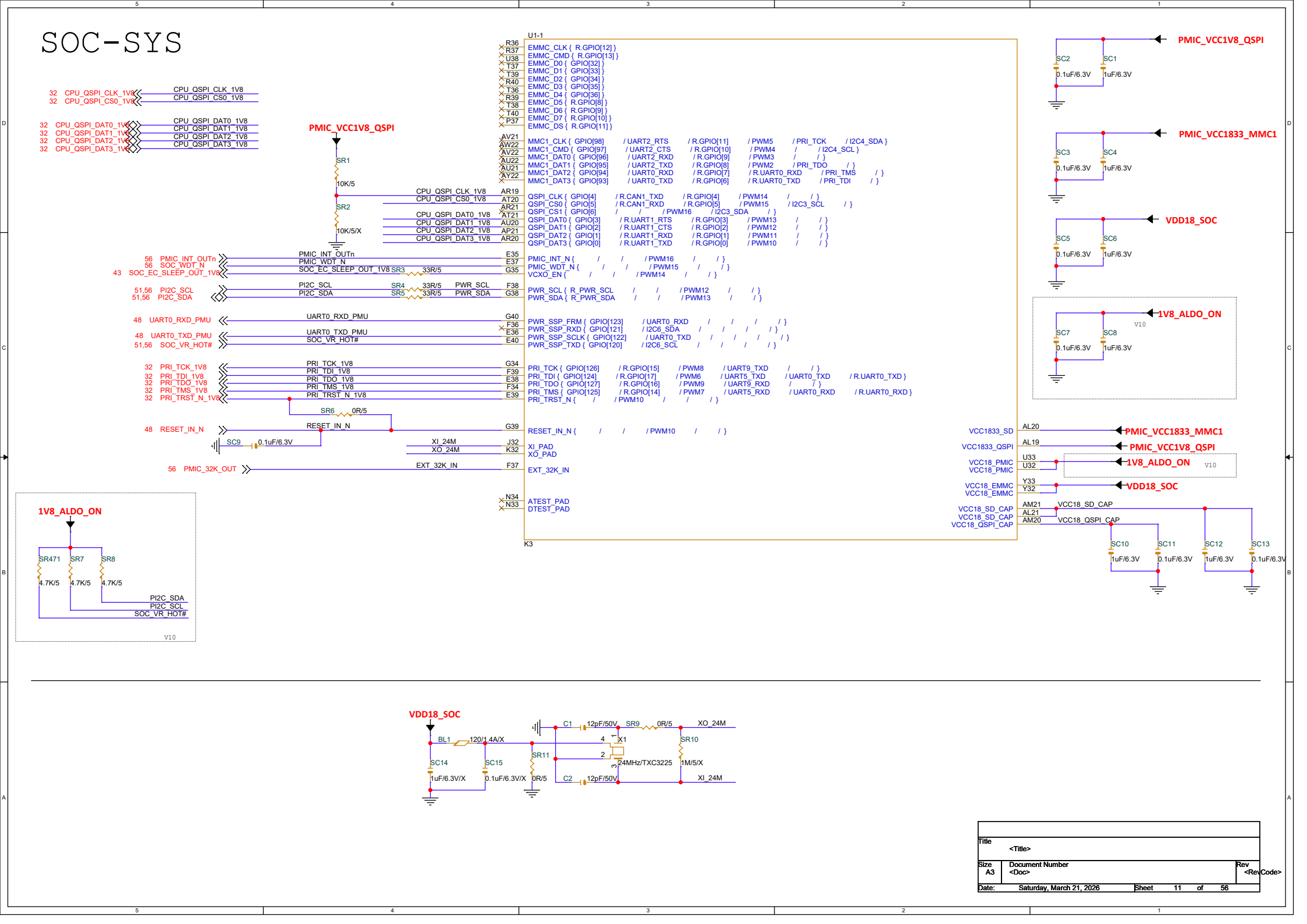
SOC-SYS



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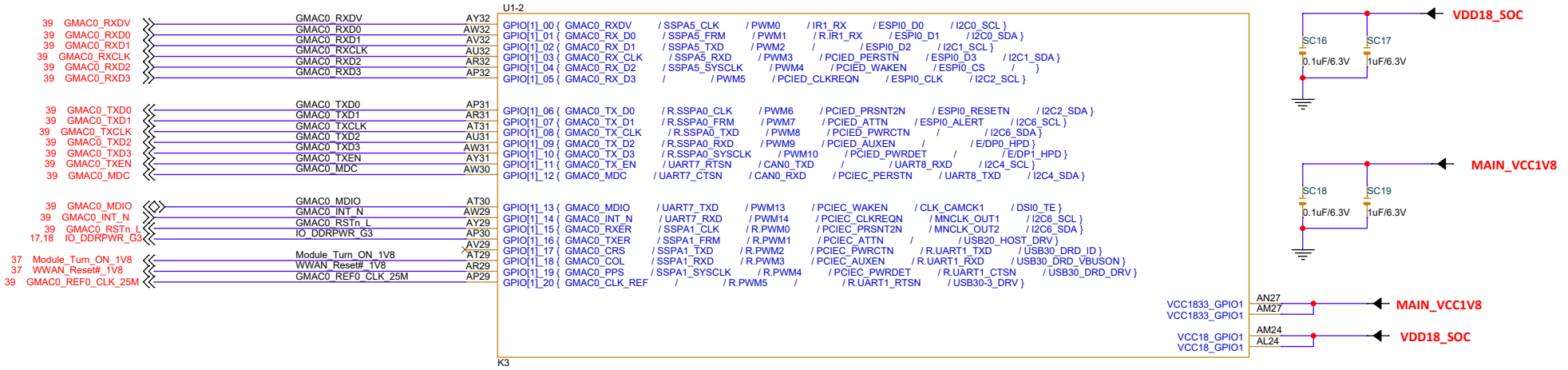
SOC-GPOIO1-GMAC0



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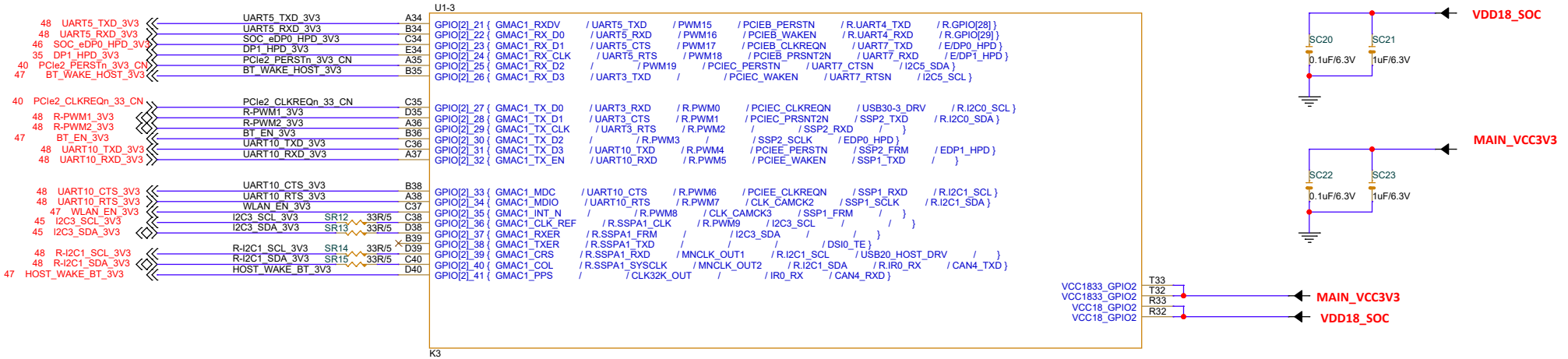
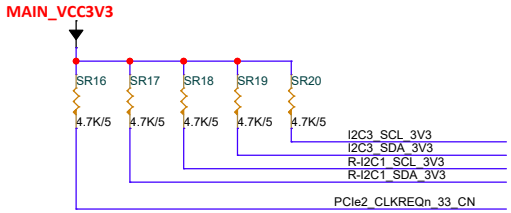
SOC-GPOIO2-GMAC1





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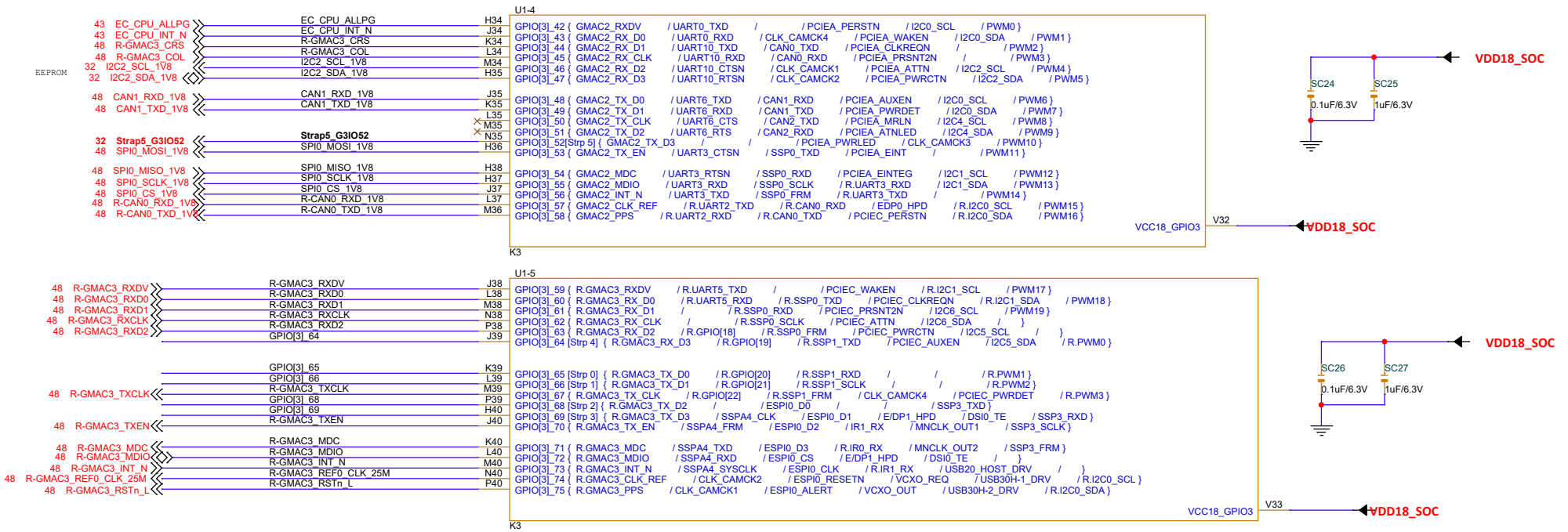
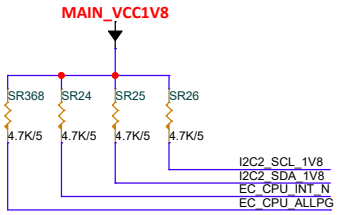
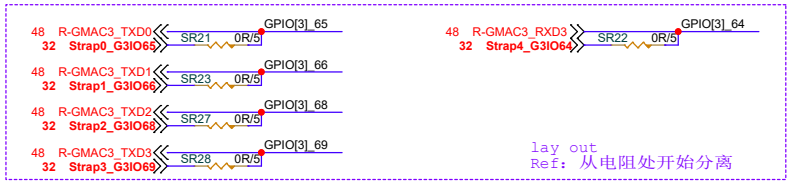
SOC-GPIO3-GMAC2/3

1.8V only







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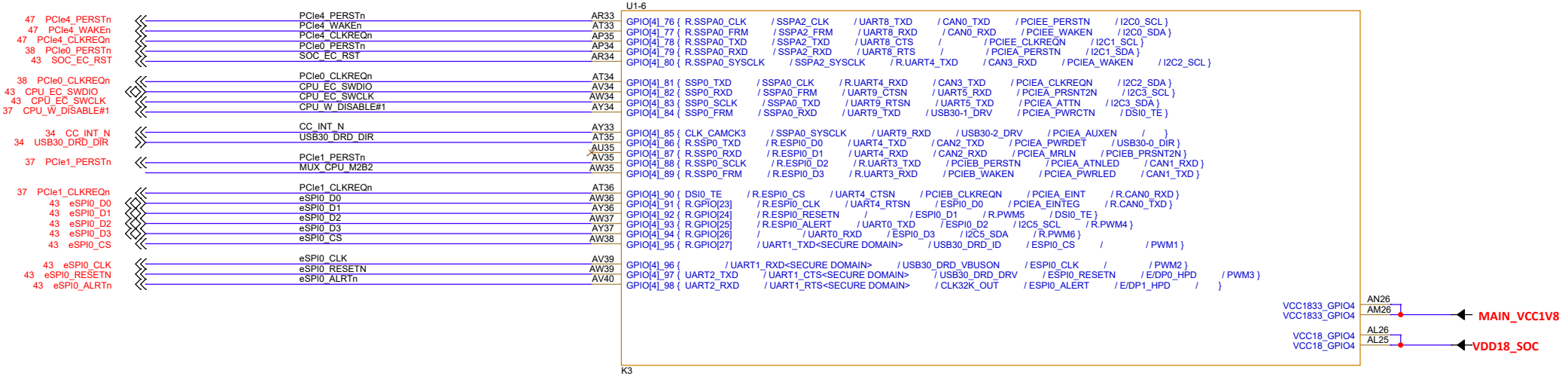
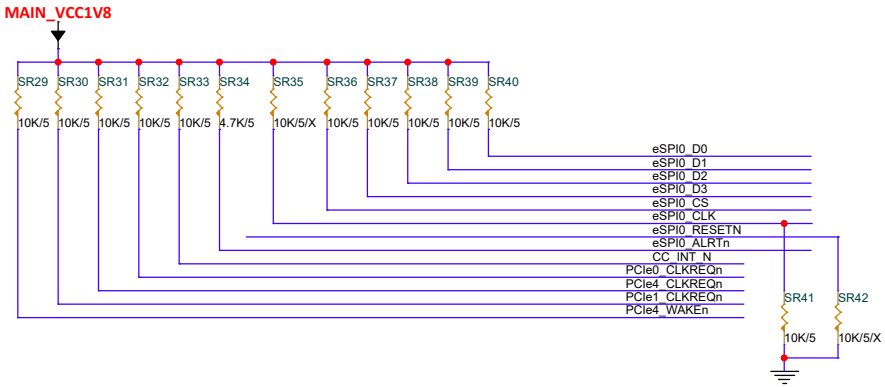
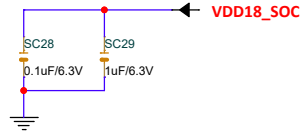
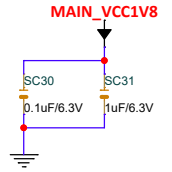
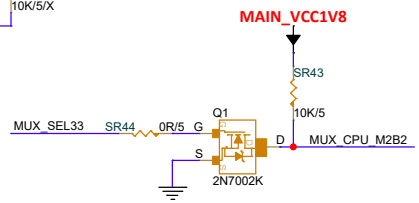
SOC-GPIO-4

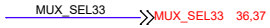












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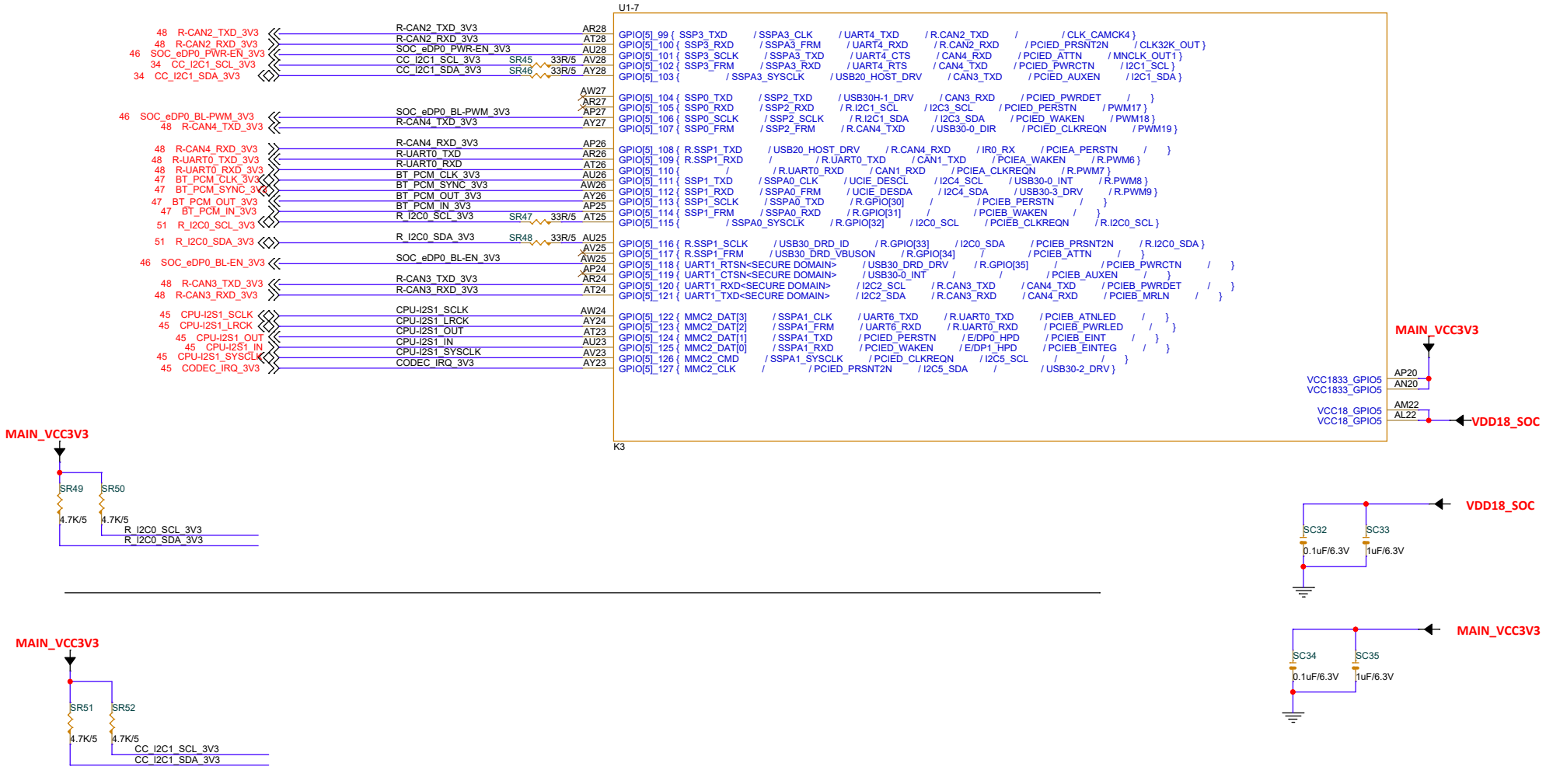
SOC-GPIO-5



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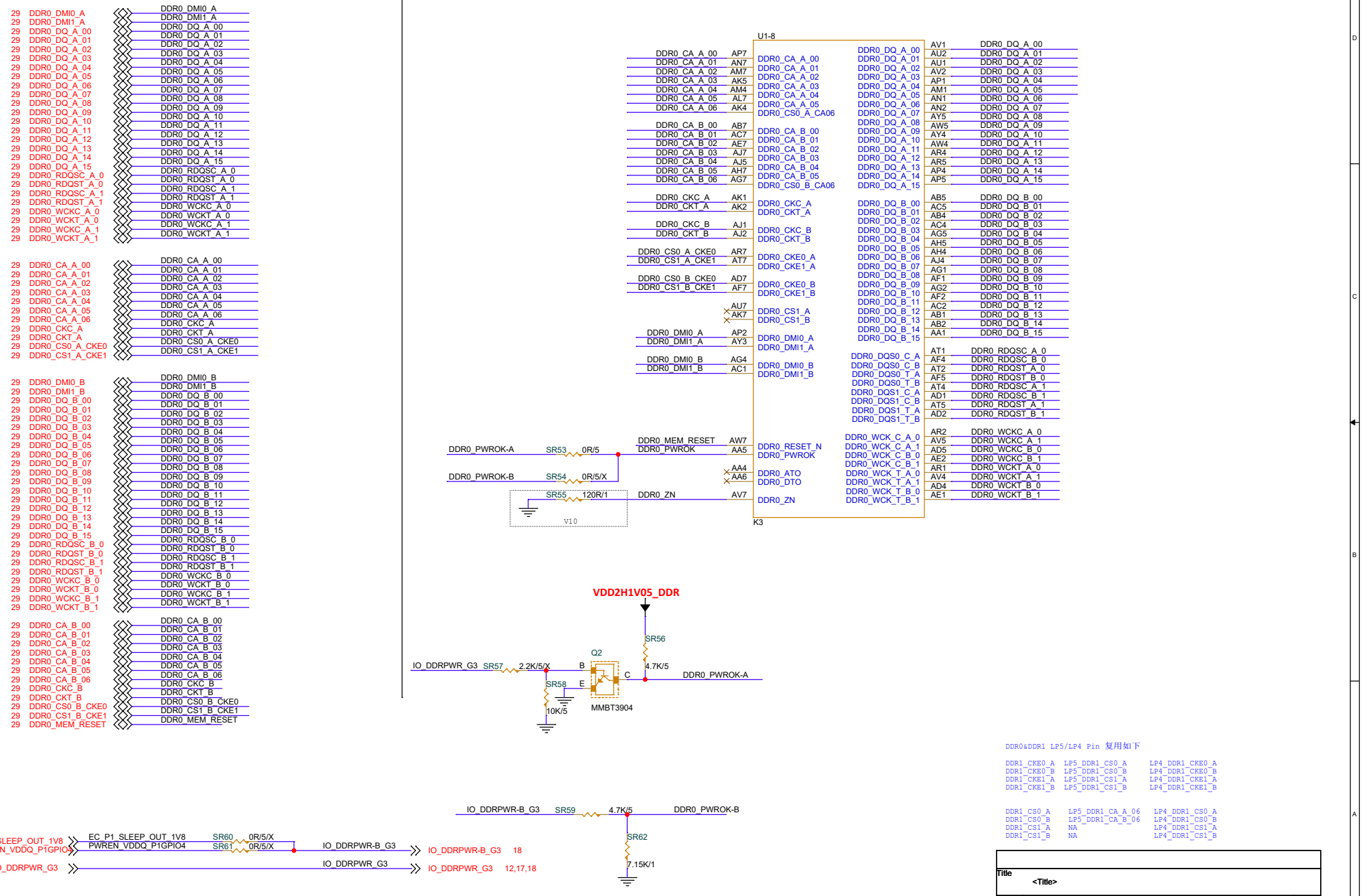
K2-DDR0


29 DDR0_DMI0_A
29 DDR0_DMI1_A
29 DDR0_DQ_A_00
29 DDR0_DQ_A_01
29 DDR0_DQ_A_02
29 DDR0_DQ_A_03
29 DDR0_DQ_A_04
29 DDR0_DQ_A_05
29 DDR0_DQ_A_06
29 DDR0_DQ_A_07
29 DDR0_DQ_A_08
29 DDR0_DQ_A_09
29 DDR0_DQ_A_10
29 DDR0_DQ_A_11
29 DDR0_DQ_A_12
29 DDR0_DQ_A_13
29 DDR0_DQ_A_14
29 DDR0_DQ_A_15
29 DDR0_RDQSC_A_0
29 DDR0_RDQST_A_0
29 DDR0_RDQSC_A_1
29 DDR0_RDQST_A_1
29 DDR0_WCKC_A_0
29 DDR0_WCKT_A_0
29 DDR0_WCKC_A_1
29 DDR0_WCKT_A_1
DDR0_DMI0_A
DDR0_DMI1_A
DDR0_DQ_A_00
DDR0_DQ_A_01
DDR0_DQ_A_02
DDR0_DQ_A_03
DDR0_DQ_A_04
DDR0_DQ_A_05
DDR0_DQ_A_06
DDR0_DQ_A_07
DDR0_DQ_A_08
DDR0_DQ_A_09
DDR0_DQ_A_10
DDR0_DQ_A_11
DDR0_DQ_A_12
DDR0_DQ_A_13
DDR0_DQ_A_14
DDR0_DQ_A_15
DDR0_RDQSC_A_0
DDR0_RDQST_A_0
DDR0_RDQSC_A_1
DDR0_RDQST_A_1
DDR0_WCKC_A_0
DDR0_WCKT_A_0
DDR0_WCKC_A_1
DDR0_WCKT_A_1
29 DDR0_CA_A_00
29 DDR0_CA_A_01
29 DDR0_CA_A_02
29 DDR0_CA_A_03
29 DDR0_CA_A_04
29 DDR0_CA_A_05
29 DDR0_CA_A_06
29 DDR0_CKC_A
29 DDR0_CKT_A
29 DDR0_CS0_A_CKE0
29 DDR0_CS1_A_CKE1
DDR0_CA_A_00
DDR0_CA_A_01
DDR0_CA_A_02
DDR0_CA_A_03
DDR0_CA_A_04
DDR0_CA_A_05
DDR0_CA_A_06
DDR0_CKC_A
DDR0_CKT_A
DDR0_CS0_A_CKE0
DDR0_CS1_A_CKE1
29 DDR0_DMI0_B
29 DDR0_DMI1_B
29 DDR0_DQ_B_00
29 DDR0_DQ_B_01
29 DDR0_DQ_B_02
29 DDR0_DQ_B_03
29 DDR0_DQ_B_04
29 DDR0_DQ_B_05
29 DDR0_DQ_B_06
29 DDR0_DQ_B_07
29 DDR0_DQ_B_08
29 DDR0_DQ_B_09
29 DDR0_DQ_B_10
29 DDR0_DQ_B_11
29 DDR0_DQ_B_12
29 DDR0_DQ_B_13
29 DDR0_DQ_B_14
29 DDR0_DQ_B_15
29 DDR0_RDQSC_B_0
29 DDR0_RDQST_B_0
29 DDR0_RDQSC_B_1
29 DDR0_RDQST_B_1
29 DDR0_WCKC_B_0
29 DDR0_WCKT_B_0
29 DDR0_WCKC_B_1
29 DDR0_WCKT_B_1
DDR0_DMI0_B
DDR0_DMI1_B
DDR0_DQ_B_00
DDR0_DQ_B_01
DDR0_DQ_B_02
DDR0_DQ_B_03
DDR0_DQ_B_04
DDR0_DQ_B_05
DDR0_DQ_B_06
DDR0_DQ_B_07
DDR0_DQ_B_08
DDR0_DQ_B_09
DDR0_DQ_B_10
DDR0_DQ_B_11
DDR0_DQ_B_12
DDR0_DQ_B_13
DDR0_DQ_B_14
DDR0_DQ_B_15
DDR0_RDQSC_B_0
DDR0_RDQST_B_0
DDR0_RDQSC_B_1
DDR0_RDQST_B_1
DDR0_WCKC_B_0
DDR0_WCKT_B_0
DDR0_WCKC_B_1
DDR0_WCKT_B_1
29 DDR0_CA_B_00
29 DDR0_CA_B_01
29 DDR0_CA_B_02
29 DDR0_CA_B_03
29 DDR0_CA_B_04
29 DDR0_CA_B_05
29 DDR0_CA_B_06
29 DDR0_CKC_B
29 DDR0_CKT_B
29 DDR0_CS0_B_CKE0
29 DDR0_CS1_B_CKE1
29 DDR0_MEM_RESET
DDR0_CA_B_00
DDR0_CA_B_01
DDR0_CA_B_02
DDR0_CA_B_03
DDR0_CA_B_04
DDR0_CA_B_05
DDR0_CA_B_06
DDR0_CKC_B
DDR0_CKT_B
DDR0_CS0_B_CKE0
DDR0_CS1_B_CKE1
DDR0_MEM_RESET
U1-8
DDR0_CA_A_00 AP7
DDR0_CA_A_01 AN7
DDR0_CA_A_02 AM7
DDR0_CA_A_03 AK5
DDR0_CA_A_04 AM4
DDR0_CA_A_05 AL7
DDR0_CA_A_06 AK4
DDR0_CA_B_00 AB7
DDR0_CA_B_01 AC7
DDR0_CA_B_02 AE7
DDR0_CA_B_03 AJ7
DDR0_CA_B_04 AJ5
DDR0_CA_B_05 AH7
DDR0_CA_B_06 AG7
DDR0_CKC_A AK1
DDR0_CKT_A AK2
DDR0_CKC_B AJ1
DDR0_CKT_B AJ2
DDR0_CS0_A_CKE0 AR7
DDR0_CS1_A_CKE1 AT7
DDR0_CS0_B_CKE0 AD7
DDR0_CS1_B_CKE1 AF7
AU7
AK7
DDR0_DMI0_A AP2
DDR0_DMI1_A AY3
DDR0_DMI0_B AG4
DDR0_DMI1_B AC1
DDR0_MEM_RESET AW7
DDR0_PWROK AA5
AA4
AA6
DDR0_ZN AV7
DDR0_CA_A_00
DDR0_CA_A_01
DDR0_CA_A_02
DDR0_CA_A_03
DDR0_CA_A_04
DDR0_CA_A_05
DDR0_CA_A_06
DDR0_CS0_A_CA06
DDR0_CA_B_00
DDR0_CA_B_01
DDR0_CA_B_02
DDR0_CA_B_03
DDR0_CA_B_04
DDR0_CA_B_05
DDR0_CS0_B_CA06
DDR0_CKC_A
DDR0_CKT_A
DDR0_CKC_B
DDR0_CKT_B
DDR0_CKE0_A
DDR0_CKE1_A
DDR0_CKE0_B
DDR0_CKE1_B
DDR0_CS1_A
DDR0_CS1_B
DDR0_DMI0_A
DDR0_DMI1_A
DDR0_DMI0_B
DDR0_DMI1_B
DDR0_RESET_N
DDR0_PWROK
DDR0_ATO
DDR0_DTO
DDR0_ZN
DDR0_DQ_A_00
DDR0_DQ_A_01
DDR0_DQ_A_02
DDR0_DQ_A_03
DDR0_DQ_A_04
DDR0_DQ_A_05
DDR0_DQ_A_06
DDR0_DQ_A_07
DDR0_DQ_A_08
DDR0_DQ_A_09
DDR0_DQ_A_10
DDR0_DQ_A_11
DDR0_DQ_A_12
DDR0_DQ_A_13
DDR0_DQ_A_14
DDR0_DQ_A_15
DDR0_DQ_B_00
DDR0_DQ_B_01
DDR0_DQ_B_02
DDR0_DQ_B_03
DDR0_DQ_B_04
DDR0_DQ_B_05
DDR0_DQ_B_06
DDR0_DQ_B_07
DDR0_DQ_B_08
DDR0_DQ_B_09
DDR0_DQ_B_10
DDR0_DQ_B_11
DDR0_DQ_B_12
DDR0_DQ_B_13
DDR0_DQ_B_14
DDR0_DQ_B_15
DDR0_DQS0_C_A
DDR0_DQS0_C_B
DDR0_DQS0_T_A
DDR0_DQS0_T_B
DDR0_DQS1_C_A
DDR0_DQS1_C_B
DDR0_DQS1_T_A
DDR0_DQS1_T_B
DDR0_WCK_C_A_0
DDR0_WCK_C_A_1
DDR0_WCK_C_B_0
DDR0_WCK_C_B_1
DDR0_WCK_T_A_0
DDR0_WCK_T_A_1
DDR0_WCK_T_B_0
DDR0_WCK_T_B_1
AV1 DDR0_DQ_A_00
AU2 DDR0_DQ_A_01
AU1 DDR0_DQ_A_02
AV2 DDR0_DQ_A_03
AP1 DDR0_DQ_A_04
AM1 DDR0_DQ_A_05
AN1 DDR0_DQ_A_06
AN2 DDR0_DQ_A_07
AY5 DDR0_DQ_A_08
AW5 DDR0_DQ_A_09
AY4 DDR0_DQ_A_10
AW4 DDR0_DQ_A_11
AR4 DDR0_DQ_A_12
AR5 DDR0_DQ_A_13
AP4 DDR0_DQ_A_14
AP5 DDR0_DQ_A_15
AB5 DDR0_DQ_B_00
AC5 DDR0_DQ_B_01
AB4 DDR0_DQ_B_02
AC4 DDR0_DQ_B_03
AG5 DDR0_DQ_B_04
AH5 DDR0_DQ_B_05
AH4 DDR0_DQ_B_06
AJ4 DDR0_DQ_B_07
AG1 DDR0_DQ_B_08
AF1 DDR0_DQ_B_09
AG2 DDR0_DQ_B_10
AF2 DDR0_DQ_B_11
AC2 DDR0_DQ_B_12
AB1 DDR0_DQ_B_13
AB2 DDR0_DQ_B_14
AA1 DDR0_DQ_B_15
AT1 DDR0_RDQSC_A_0
AF4 DDR0_RDQSC_B_0
AT2 DDR0_RDQST_A_0
AF5 DDR0_RDQST_B_0
AT4 DDR0_RDQSC_A_1
AD1 DDR0_RDQSC_B_1
AT5 DDR0_RDQST_A_1
AD2 DDR0_RDQST_B_1
AR2 DDR0_WCKC_A_0
AV5 DDR0_WCKC_A_1
AD5 DDR0_WCKC_B_0
AE2 DDR0_WCKC_B_1
AR1 DDR0_WCKT_A_0
AV4 DDR0_WCKT_A_1
AD4 DDR0_WCKT_B_0
AE1 DDR0_WCKT_B_1
K3
DDR0_PWROK-A SR53 0R/5
DDR0_PWROK-B SR54 0R/5/X
SR55 120R/1
V10
VDD2H1V05_DDR
SR56
4.7K/5
Q2
IO_DDRPWR_G3 SR57 2.2K/5/X
B
C
DDR0_PWROK-A
SR58
E
10K/5
MMBT3904
IO_DDRPWR-B_G3 SR59 4.7K/5
DDR0_PWROK-B
SR62
7.15K/1
43,56 EC_P1_SLEEP_OUT_1V8
56 PWREN_VDDQ_P1GPIO4
EC_P1_SLEEP_OUT_1V8 SR60 0R/5/X
PWREN_VDDQ_P1GPIO4 SR61 0R/5/X
IO_DDRPWR-B_G3
IO_DDRPWR-B_G3 18
12,17,18 IO_DDRPWR_G3
IO_DDRPWR_G3
IO_DDRPWR_G3 12,17,18
DDR0&DDR1 LP5/LP4 Pin 复用如下
DDR1_CKE0_A LP5_DDR1_CS0_A LP4_DDR1_CKE0_A
DDR1_CKE0_B LP5_DDR1_CS0_B LP4_DDR1_CKE0_B
DDR1_CKE1_A LP5_DDR1_CS1_A LP4_DDR1_CKE1_A
DDR1_CKE1_B LP5_DDR1_CS1_B LP4_DDR1_CKE1_B
DDR1_CS0_A LP5_DDR1_CA_A_06 LP4_DDR1_CS0_A
DDR1_CS0_B LP5_DDR1_CA_B_06 LP4_DDR1_CS0_B
DDR1_CS1_A NA LP4_DDR1_CS1_A
DDR1_CS1_B NA LP4_DDR1_CS1_B
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<Title>
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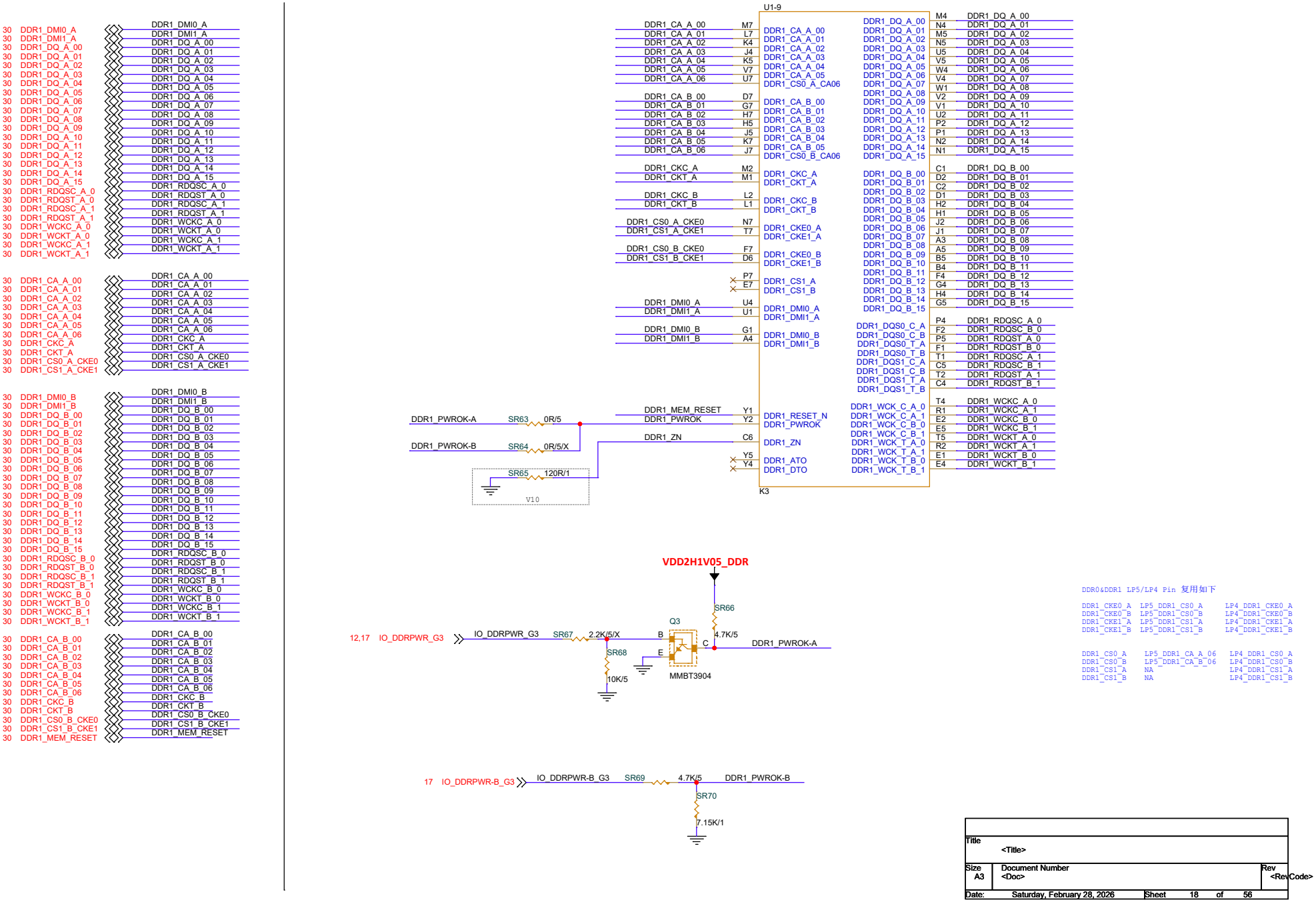
K2-DDR1


30 DDR1_DMI0_A
30 DDR1_DMI1_A
30 DDR1_DQ_A_00
30 DDR1_DQ_A_01
30 DDR1_DQ_A_02
30 DDR1_DQ_A_03
30 DDR1_DQ_A_04
30 DDR1_DQ_A_05
30 DDR1_DQ_A_06
30 DDR1_DQ_A_07
30 DDR1_DQ_A_08
30 DDR1_DQ_A_09
30 DDR1_DQ_A_10
30 DDR1_DQ_A_11
30 DDR1_DQ_A_12
30 DDR1_DQ_A_13
30 DDR1_DQ_A_14
30 DDR1_DQ_A_15
30 DDR1_RDQSC_A_0
30 DDR1_RDQST_A_0
30 DDR1_RDQSC_A_1
30 DDR1_RDQST_A_1
30 DDR1_WCKC_A_0
30 DDR1_WCKT_A_0
30 DDR1_WCKC_A_1
30 DDR1_WCKT_A_1
DDR1_DMI0_A
DDR1_DMI1_A
DDR1_DQ_A_00
DDR1_DQ_A_01
DDR1_DQ_A_02
DDR1_DQ_A_03
DDR1_DQ_A_04
DDR1_DQ_A_05
DDR1_DQ_A_06
DDR1_DQ_A_07
DDR1_DQ_A_08
DDR1_DQ_A_09
DDR1_DQ_A_10
DDR1_DQ_A_11
DDR1_DQ_A_12
DDR1_DQ_A_13
DDR1_DQ_A_14
DDR1_DQ_A_15
DDR1_RDQSC_A_0
DDR1_RDQST_A_0
DDR1_RDQSC_A_1
DDR1_RDQST_A_1
DDR1_WCKC_A_0
DDR1_WCKT_A_0
DDR1_WCKC_A_1
DDR1_WCKT_A_1
30 DDR1_CA_A_00
30 DDR1_CA_A_01
30 DDR1_CA_A_02
30 DDR1_CA_A_03
30 DDR1_CA_A_04
30 DDR1_CA_A_05
30 DDR1_CA_A_06
30 DDR1_CKC_A
30 DDR1_CKT_A
30 DDR1_CS0_A_CKE0
30 DDR1_CS1_A_CKE1
DDR1_CA_A_00
DDR1_CA_A_01
DDR1_CA_A_02
DDR1_CA_A_03
DDR1_CA_A_04
DDR1_CA_A_05
DDR1_CA_A_06
DDR1_CKC_A
DDR1_CKT_A
DDR1_CS0_A_CKE0
DDR1_CS1_A_CKE1
30 DDR1_DMI0_B
30 DDR1_DMI1_B
30 DDR1_DQ_B_00
30 DDR1_DQ_B_01
30 DDR1_DQ_B_02
30 DDR1_DQ_B_03
30 DDR1_DQ_B_04
30 DDR1_DQ_B_05
30 DDR1_DQ_B_06
30 DDR1_DQ_B_07
30 DDR1_DQ_B_08
30 DDR1_DQ_B_09
30 DDR1_DQ_B_10
30 DDR1_DQ_B_11
30 DDR1_DQ_B_12
30 DDR1_DQ_B_13
30 DDR1_DQ_B_14
30 DDR1_DQ_B_15
30 DDR1_RDQSC_B_0
30 DDR1_RDQST_B_0
30 DDR1_RDQSC_B_1
30 DDR1_RDQST_B_1
30 DDR1_WCKC_B_0
30 DDR1_WCKT_B_0
30 DDR1_WCKC_B_1
30 DDR1_WCKT_B_1
DDR1_DMI0_B
DDR1_DMI1_B
DDR1_DQ_B_00
DDR1_DQ_B_01
DDR1_DQ_B_02
DDR1_DQ_B_03
DDR1_DQ_B_04
DDR1_DQ_B_05
DDR1_DQ_B_06
DDR1_DQ_B_07
DDR1_DQ_B_08
DDR1_DQ_B_09
DDR1_DQ_B_10
DDR1_DQ_B_11
DDR1_DQ_B_12
DDR1_DQ_B_13
DDR1_DQ_B_14
DDR1_DQ_B_15
DDR1_RDQSC_B_0
DDR1_RDQST_B_0
DDR1_RDQSC_B_1
DDR1_RDQST_B_1
DDR1_WCKC_B_0
DDR1_WCKT_B_0
DDR1_WCKC_B_1
DDR1_WCKT_B_1
30 DDR1_CA_B_00
30 DDR1_CA_B_01
30 DDR1_CA_B_02
30 DDR1_CA_B_03
30 DDR1_CA_B_04
30 DDR1_CA_B_05
30 DDR1_CA_B_06
30 DDR1_CKC_B
30 DDR1_CKT_B
30 DDR1_CS0_B_CKE0
30 DDR1_CS1_B_CKE1
30 DDR1_MEM_RESET
DDR1_CA_B_00
DDR1_CA_B_01
DDR1_CA_B_02
DDR1_CA_B_03
DDR1_CA_B_04
DDR1_CA_B_05
DDR1_CA_B_06
DDR1_CKC_B
DDR1_CKT_B
DDR1_CS0_B_CKE0
DDR1_CS1_B_CKE1
DDR1_MEM_RESET
U1-9
DDR1_CA_A_00 M7
DDR1_CA_A_01 L7
DDR1_CA_A_02 K4
DDR1_CA_A_03 J4
DDR1_CA_A_04 K5
DDR1_CA_A_05 V7
DDR1_CA_A_06 U7
DDR1_CA_B_00 D7
DDR1_CA_B_01 G7
DDR1_CA_B_02 H7
DDR1_CA_B_03 H5
DDR1_CA_B_04 J5
DDR1_CA_B_05 K7
DDR1_CA_B_06 J7
DDR1_CKC_A M2
DDR1_CKT_A M1
DDR1_CKC_B L2
DDR1_CKT_B L1
DDR1_CS0_A_CKE0 N7
DDR1_CS1_A_CKE1 T7
DDR1_CS0_B_CKE0 F7
DDR1_CS1_B_CKE1 D6
P7
E7
DDR1_DMI0_A U4
DDR1_DMI1_A U1
DDR1_DMI0_B G1
DDR1_DMI1_B A4
DDR1_MEM_RESET Y1
DDR1_PWROK Y2
DDR1_ZN C6
Y5
Y4
DDR1_CA_A_00
DDR1_CA_A_01
DDR1_CA_A_02
DDR1_CA_A_03
DDR1_CA_A_04
DDR1_CA_A_05
DDR1_CA_A_06
DDR1_CS0_A_CA06
DDR1_CA_B_00
DDR1_CA_B_01
DDR1_CA_B_02
DDR1_CA_B_03
DDR1_CA_B_04
DDR1_CA_B_05
DDR1_CA_B_06
DDR1_CS0_B_CA06
DDR1_CKC_A
DDR1_CKT_A
DDR1_CKC_B
DDR1_CKT_B
DDR1_CKE0_A
DDR1_CKE1_A
DDR1_CKE0_B
DDR1_CKE1_B
DDR1_CS1_A
DDR1_CS1_B
DDR1_DMI0_A
DDR1_DMI1_A
DDR1_DMI0_B
DDR1_DMI1_B
DDR1_RESET_N
DDR1_PWROK
DDR1_ZN
DDR1_ATO
DDR1_DTO
DDR1_DQ_A_00 M4
DDR1_DQ_A_01 N4
DDR1_DQ_A_02 M5
DDR1_DQ_A_03 N5
DDR1_DQ_A_04 U5
DDR1_DQ_A_05 V5
DDR1_DQ_A_06 W4
DDR1_DQ_A_07 V4
DDR1_DQ_A_08 W1
DDR1_DQ_A_09 V2
DDR1_DQ_A_10 V1
DDR1_DQ_A_11 U2
DDR1_DQ_A_12 P2
DDR1_DQ_A_13 P1
DDR1_DQ_A_14 N2
DDR1_DQ_A_15 N1
DDR1_DQ_B_00 C1
DDR1_DQ_B_01 D2
DDR1_DQ_B_02 C2
DDR1_DQ_B_03 D1
DDR1_DQ_B_04 H2
DDR1_DQ_B_05 H1
DDR1_DQ_B_06 J2
DDR1_DQ_B_07 J1
DDR1_DQ_B_08 A3
DDR1_DQ_B_09 A5
DDR1_DQ_B_10 B5
DDR1_DQ_B_11 B4
DDR1_DQ_B_12 F4
DDR1_DQ_B_13 G4
DDR1_DQ_B_14 H4
DDR1_DQ_B_15 G5
DDR1_DQS0_C_A P4
DDR1_DQS0_C_B F2
DDR1_DQS0_T_A P5
DDR1_DQS0_T_B F1
DDR1_DQS1_C_A T1
DDR1_DQS1_C_B C5
DDR1_DQS1_T_A T2
DDR1_DQS1_T_B C4
DDR1_WCK_C_A_0 T4
DDR1_WCK_C_A_1 R1
DDR1_WCK_C_B_0 E2
DDR1_WCK_C_B_1 E5
DDR1_WCK_T_A_0 T5
DDR1_WCK_T_A_1 R2
DDR1_WCK_T_B_0 E1
DDR1_WCK_T_B_1 E4
DDR1_RDQSC_A_0
DDR1_RDQSC_B_0
DDR1_RDQST_A_0
DDR1_RDQST_B_0
DDR1_RDQSC_A_1
DDR1_RDQSC_B_1
DDR1_RDQST_A_1
DDR1_RDQST_B_1
DDR1_WCKC_A_0
DDR1_WCKC_A_1
DDR1_WCKC_B_0
DDR1_WCKC_B_1
DDR1_WCKT_A_0
DDR1_WCKT_A_1
DDR1_WCKT_B_0
DDR1_WCKT_B_1
K3
DDR1_PWROK-A
SR63 0R/5
DDR1_PWROK-B
SR64 0R/5/X
SR65 120R/1
V10
VDD2H1V05_DDR
SR66
4.7K/5
Q3
MMBT3904
12,17 IO_DDRPWR_G3
IO_DDRPWR_G3
SR67 2.2K/5/X
SR68
10K/5
B
E
C
DDR1_PWROK-A
17 IO_DDRPWR-B_G3
IO_DDRPWR-B_G3
SR69 4.7K/5
DDR1_PWROK-B
SR70
7.15K/1
DDR0&DDR1 LP5/LP4 Pin 复用如下
DDR1_CKE0_A LP5_DDR1_CS0_A LP4_DDR1_CKE0_A
DDR1_CKE0_B LP5_DDR1_CS0_B LP4_DDR1_CKE0_B
DDR1_CKE1_A LP5_DDR1_CS1_A LP4_DDR1_CKE1_A
DDR1_CKE1_B LP5_DDR1_CS1_B LP4_DDR1_CKE1_B
DDR1_CS0_A LP5_DDR1_CA_A_06 LP4_DDR1_CS0_A
DDR1_CS0_B LP5_DDR1_CA_B_06 LP4_DDR1_CS0_B
DDR1_CS1_A NA LP4_DDR1_CS1_A
DDR1_CS1_B NA LP4_DDR1_CS1_B
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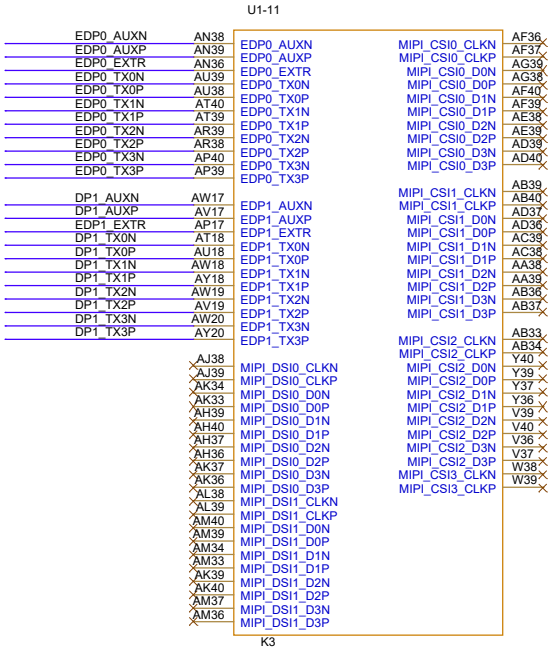
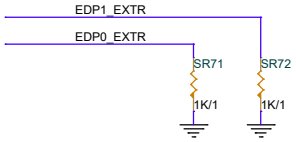
Media





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UCIE/UFS

31 UFS_REF_CLK
31 UFS_RST_N
31 UFS_RXD0N
31 UFS_RXD0P
31 UFS_RXD1N
31 UFS_RXD1P

UFS_REF_CLK
UFS_RST_N
UFS_RXD0N
UFS_RXD0P
UFS_RXD1N
UFS_RXD1P

31 UFS_TXD0N
31 UFS_TXD0P
31 UFS_TXD1N
31 UFS_TXD1P

UFS_TXD0N
UFS_TXD0P
UFS_TXD1N
UFS_TXD1P

U1-12

H26	UCIE_BGR_EAREFCLKN
J26	UCIE_BGR_EAREFCLKP
H25	UCIE_EW_ATEST
E24	UCIE_EW_O_CKNT
F24	UCIE_EW_O_CKPT
B29	UCIE_EW_RXCKN_M0
A28	UCIE_EW_RXCKP_M0
A29	UCIE_EW_RXCKSB_M0
G32	UCIE_EW_RXDATA_M0[0]
D32	UCIE_EW_RXDATA_M0[1]
D28	UCIE_EW_RXDATA_M0[10]
C28	UCIE_EW_RXDATA_M0[11]
C30	UCIE_EW_RXDATA_M0[12]
G29	UCIE_EW_RXDATA_M0[13]
D29	UCIE_EW_RXDATA_M0[14]
B30	UCIE_EW_RXDATA_M0[15]
A32	UCIE_EW_RXDATA_M0[2]
F31	UCIE_EW_RXDATA_M0[3]
G31	UCIE_EW_RXDATA_M0[4]
B32	UCIE_EW_RXDATA_M0[5]
D31	UCIE_EW_RXDATA_M0[6]
A31	UCIE_EW_RXDATA_M0[7]
E29	UCIE_EW_RXDATA_M0[8]
E30	UCIE_EW_RXDATA_M0[9]
E32	UCIE_EW_RXDATASB_M0
C31	UCIE_EW_RXTRK_M0
F30	UCIE_EW_RXVLD_M0
A25	UCIE_EW_TXCKN_M0
B26	UCIE_EW_TXCKP_M0
E26	UCIE_EW_TXCKSB_M0
D23	UCIE_EW_TXDATA_M0[0]
G26	UCIE_EW_TXDATA_M0[1]
G28	UCIE_EW_TXDATA_M0[10]
C27	UCIE_EW_TXDATA_M0[11]
D26	UCIE_EW_TXDATA_M0[12]
E27	UCIE_EW_TXDATA_M0[13]
B27	UCIE_EW_TXDATA_M0[14]
F28	UCIE_EW_TXDATA_M0[15]
A23	UCIE_EW_TXDATA_M0[2]
B24	UCIE_EW_TXDATA_M0[3]
C24	UCIE_EW_TXDATA_M0[4]
B23	UCIE_EW_TXDATA_M0[5]
G25	UCIE_EW_TXDATA_M0[6]
F25	UCIE_EW_TXDATA_M0[7]
A26	UCIE_EW_TXDATA_M0[8]
F27	UCIE_EW_TXDATA_M0[9]
E23	UCIE_EW_TXDATASB_M0
C25	UCIE_EW_TXTRK_M0
D25	UCIE_EW_TXVLD_M0
H28	UCIE_EW_VCTRL_EXT

UFS_REF_CLK — SR73 0R/5 — AR17 — UFS_REF_CLK
UFS_RST_N — AV13 — UFS_RST_N
UFS_RXD0N — AW16 — UFS_RXD0N
UFS_RXD0P — AY16 — UFS_RXD0P
UFS_RXD1N — AY14 — UFS_RXD1N
UFS_RXD1P — AW14 — UFS_RXD1P
UFS_TXD0N — AT16 — UFS_TXD0N
UFS_TXD0P — AU16 — UFS_TXD0P
UFS_TXD1N — AV15 — UFS_TXD1N
UFS_TXD1P — AW15 — UFS_TXD1P

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PCIE/USB

38 PCIe0_RX0n
38 PCIe0_RX0p
38 PCIe0_TX0n
38 PCIe0_TX0p
38 PCIe0_RX1n
38 PCIe0_RX1p
38 PCIe0_TX1n
38 PCIe0_TX1p
38 PCIe0_REFCLK_n
38 PCIe0_REFCLK_P

PCIe0_RX0n
PCIe0_RX0p
PCIe0_TX0n
PCIe0_TX0p
PCIe0_RX1n
PCIe0_RX1p
PCIe0_TX1n
PCIe0_TX1p
PCIe0_REFCLK_n
PCIe0_REFCLK_P

36 PCIe1_RX0n
36 PCIe1_RX0p
36 PCIe1_TX0n
36 PCIe1_TX0p
36 PCIe1_RX1n
36 PCIe1_RX1p
36 PCIe1_TX1n
36 PCIe1_TX1p
37 PCIe1_REFCLK_n
37 PCIe1_REFCLK_p

PCIe1_RX0n
PCIe1_RX0p
PCIe1_TX0n
PCIe1_TX0p
PCIe1_RX1n
PCIe1_RX1p
PCIe1_TX1n
PCIe1_TX1p
PCIe1_REFCLK_n
PCIe1_REFCLK_p

40 PCIe2_RX0n
40 PCIe2_RX0p
40 PCIe2_TX0n
40 PCIe2_TX0p
40 PCIe3_RX0n
40 PCIe3_RX0p
40 PCIe3_TX0n
40 PCIe3_TX0p
40 PCIe2_REFCLK_n
40 PCIe2_REFCLK_p

PCIe2_RX0n
PCIe2_RX0p
PCIe2_TX0n
PCIe2_TX0p
PCIe3_RX0n
PCIe3_RX0p
PCIe3_TX0n
PCIe3_TX0p
PCIe2_REFCLK_n
PCIe2_REFCLK_p

35 USB3-D_0_RX0n
35 USB3-D_0_RX0p
35 USB3-D_0_TX0n
35 USB3-D_0_TX0p

USB3-D_0_RX0n
USB3-D_0_RX0p
USB3-D_0_TX0n
USB3-D_0_TX0p

47 PCIe5_RX0n
47 PCIe5_RX0p
47 PCIe5_TX0n
47 PCIe5_TX0p
47 PCIe5_REFCLK_n
47 PCIe5_REFCLK_p

PCIe5_RX0n
PCIe5_RX0p
PCIe5_TX0n
PCIe5_TX0p
PCIe5_REFCLK_n
PCIe5_REFCLK_p

33 USB20_HOST_M
33 USB20_HOST_P

USB20_HOST_M
USB20_HOST_P

37 USB20_B_USB_M
37 USB20_B_USB_P

USB20_B_USB_M
USB20_B_USB_P

47 USB20_C_USB_M
47 USB20_C_USB_P

USB20_C_USB_M
USB20_C_USB_P

35 USB20_D_USB_M
35 USB20_D_USB_P

USB20_D_USB_M
USB20_D_USB_P

34 USB20_A_DRD_USB_M
34 USB20_A_DRD_USB_P

USB20_A_DRD_USB_M
USB20_A_DRD_USB_P

34 USB_DRD_RX1N
34 USB_DRD_RX1P
34 USB_DRD_TX1N
34 USB_DRD_TX1P

USB30_A_DRD0_RXN
USB30_A_DRD0_RXP
USB30_A_DRD0_TXN
USB30_A_DRD0_TXP

34 USB_DRD_RX2N
34 USB_DRD_RX2P
34 USB_DRD_TX2N
34 USB_DRD_TX2P

USB30_A_DRD1_RXN
USB30_A_DRD1_RXP
USB30_A_DRD1_TXN
USB30_A_DRD1_TXP

U1-10

PCIe0_RX0n G22 — PCIE0_RX0N
PCIe0_RX0p F22 — PCIE0_RX0P
PCIe0_TX0n A21 — PCIE0_TX0N
PCIe0_TX0p B21 — PCIE0_TX0P
PCIe0_RX1n E21 — PCIE0_RX1N
PCIe0_RX1p D21 — PCIE0_RX1P
PCIe0_TX1n B19 — PCIE0_TX1N
PCIe0_TX1p A19 — PCIE0_TX1P
PCIe0_REFCLK_n C20 — PCIE0_REFCLK_N
PCIe0_REFCLK_P B20 — PCIE0_REFCLK_P

PCIe1_RX0n E19 — PCIE1_RX0N
PCIe1_RX0p D19 — PCIE1_RX0P
PCIe1_TX0n A17 — PCIE1_TX0N
PCIe1_TX0p B17 — PCIE1_TX0P
PCIe1_RX1n F18 — PCIE1_RX1N
PCIe1_RX1p G18 — PCIE1_RX1P
PCIe1_TX1n B15 — PCIE1_TX1N
PCIe1_TX1p A15 — PCIE1_TX1P
PCIe1_REFCLK_n C16 — PCIE1_REFCLK_N
PCIe1_REFCLK_p B16 — PCIE1_REFCLK_P

PCIe2_RX0n E17 — PCIE2/USB3-B_RX0N
PCIe2_RX0p D17 — PCIE2/USB3-B_RX0P
PCIe2_TX0n A13 — PCIE2/USB3-B_TX0N
PCIe2_TX0p B13 — PCIE2/USB3-B_TX0P
PCIe2_REFCLK_n C14 — PCIE2_REFCLK_N
PCIe2_REFCLK_p B14 — PCIE2_REFCLK_P

PCIe3_RX0n D15 — PCIE3/USB3-C_RX0N
PCIe3_RX0p E15 — PCIE3/USB3-C_RX0P
PCIe3_TX0n A11 — PCIE3/USB3-C_TX0N
PCIe3_TX0p B11 — PCIE3/USB3-C_TX0P
B12 — PCIE3_REFCLK_N
C12 — PCIE3_REFCLK_P

USB3-D_0_RX0n D13 — PCIE4/USB3-D_RX0N
USB3-D_0_RX0p E13 — PCIE4/USB3-D_RX0P
USB3-D_0_TX0n A9 — PCIE4/USB3-D_TX0N
USB3-D_0_TX0p B9 — PCIE4/USB3-D_TX0P
C10 — PCIE4_REFCLK_N
B10 — PCIE4_REFCLK_P

PCIe5_RX0n E9 — PCIE5_RX0N
PCIe5_RX0p D9 — PCIE5_RX0P
PCIe5_TX0n A7 — PCIE5_TX0N
PCIe5_TX0p B7 — PCIE5_TX0P
PCIe5_REFCLK_n B8 — PCIE5_REFCLK_N
PCIe5_REFCLK_p C8 — PCIE5_REFCLK_P

USB20_A_DRD_USB_M AU14 — USB20_A_DRD_USB_M
USB20_A_DRD_USB_P AT14 — USB20_A_DRD_USB_P
USB20_B_USB_M C18 — USB20_B_USB_M
USB20_B_USB_P B18 — USB20_B_USB_P
USB20_C_USB_M F16 — USB20_C_USB_M
USB20_C_USB_P G16 — USB20_C_USB_P
USB20_D_USB_M E11 — USB20_D_USB_M
USB20_D_USB_P D11 — USB20_D_USB_P
USB20_HOST_M B22 — USB20_HOST_M
USB20_HOST_P C22 — USB20_HOST_P

USB30_A_DRD0_RXN AT12 — USB30_A_DRD0_RXN
USB30_A_DRD0_RXP AU12 — USB30_A_DRD0_RXP
USB30_A_DRD0_TXN AY10 — USB30_A_DRD0_TXN
USB30_A_DRD0_TXP AW10 — USB30_A_DRD0_TXP
USB30_A_DRD1_RXN AW11 — USB30_A_DRD1_RXN
USB30_A_DRD1_RXP AV11 — USB30_A_DRD1_RXP
USB30_A_DRD1_TXN AW12 — USB30_A_DRD1_TXN
USB30_A_DRD1_TXP AY12 — USB30_A_DRD1_TXP

PMIC_VCC0V8_PLL — SR74 240R/1 — PCIE/USB3_RCAL U22 — PCIE/USB3_RCAL
DC calibration Res, external 240ohm to AVDD08_OSC; Layout DC parasitic resistance less than 1ohm
F14 — PCIE_USB_COMBO_ADTEST_0
H15 — PCIE_USB_COMBO_ADTEST_1
AT10 — USB_PORTA_ADTEST

K3

Title <Title>			
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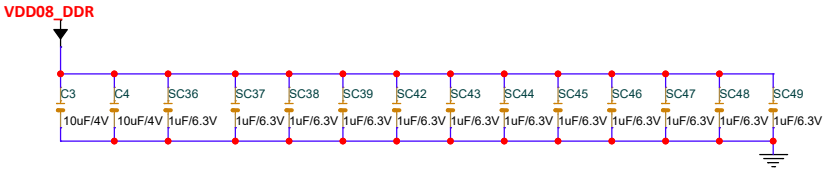
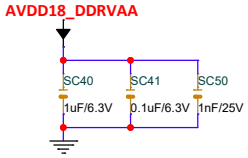
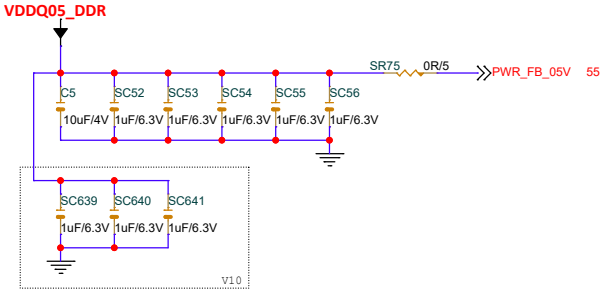
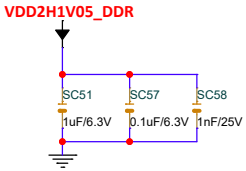
DDR PWR CAP

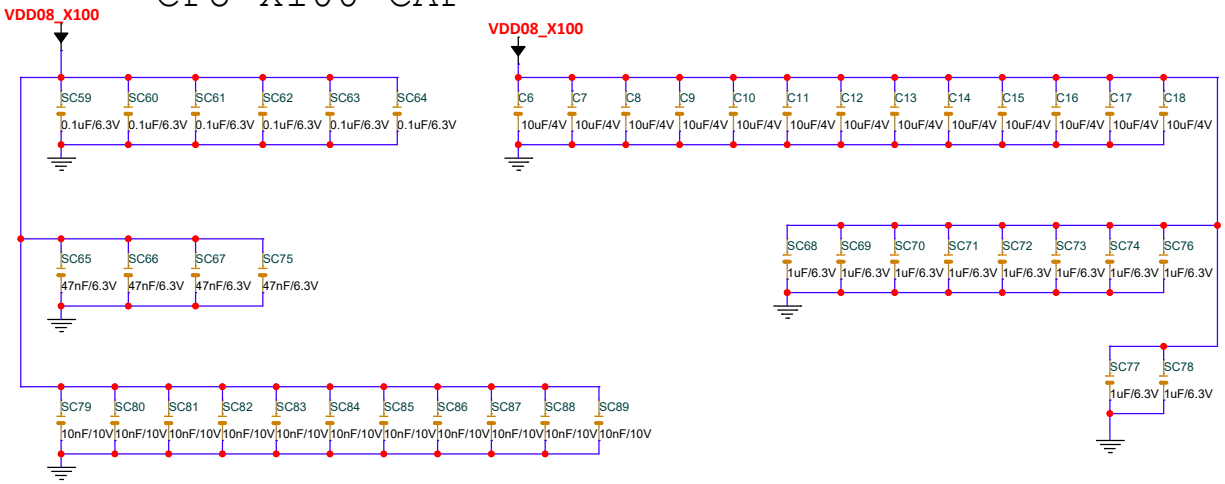


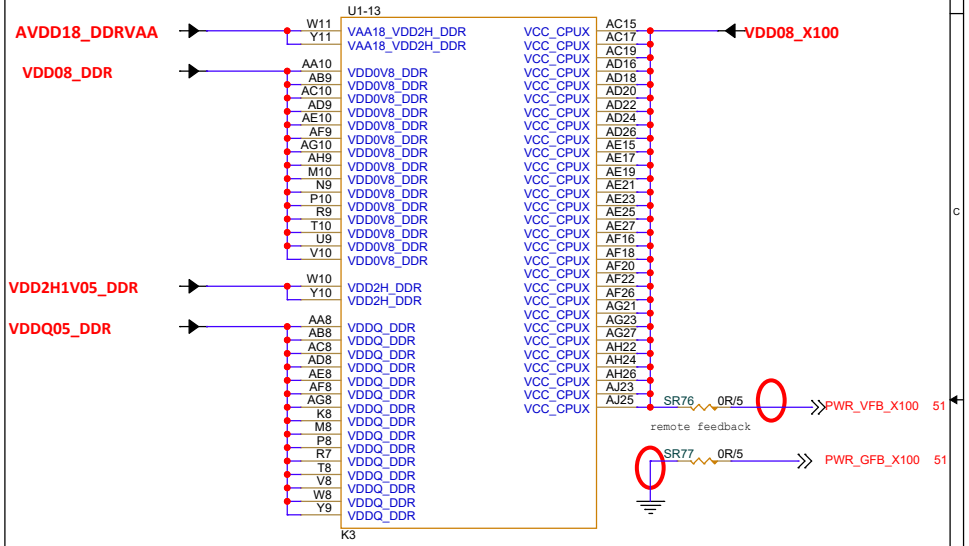






CPU X100 CAP





Title	<Title>	
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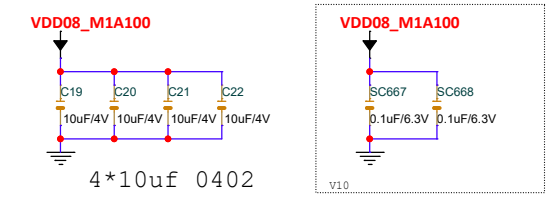
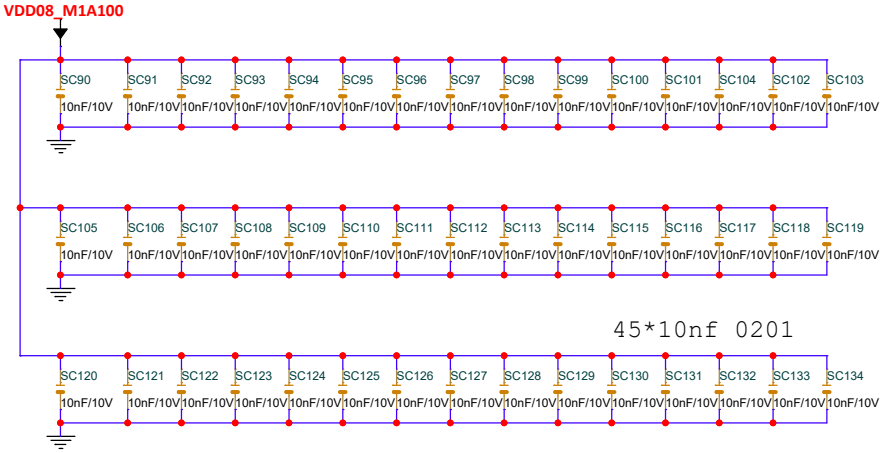
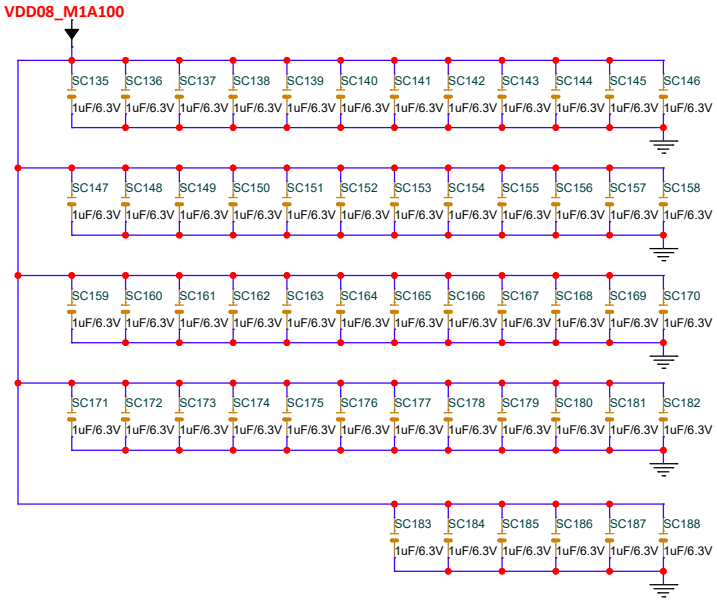
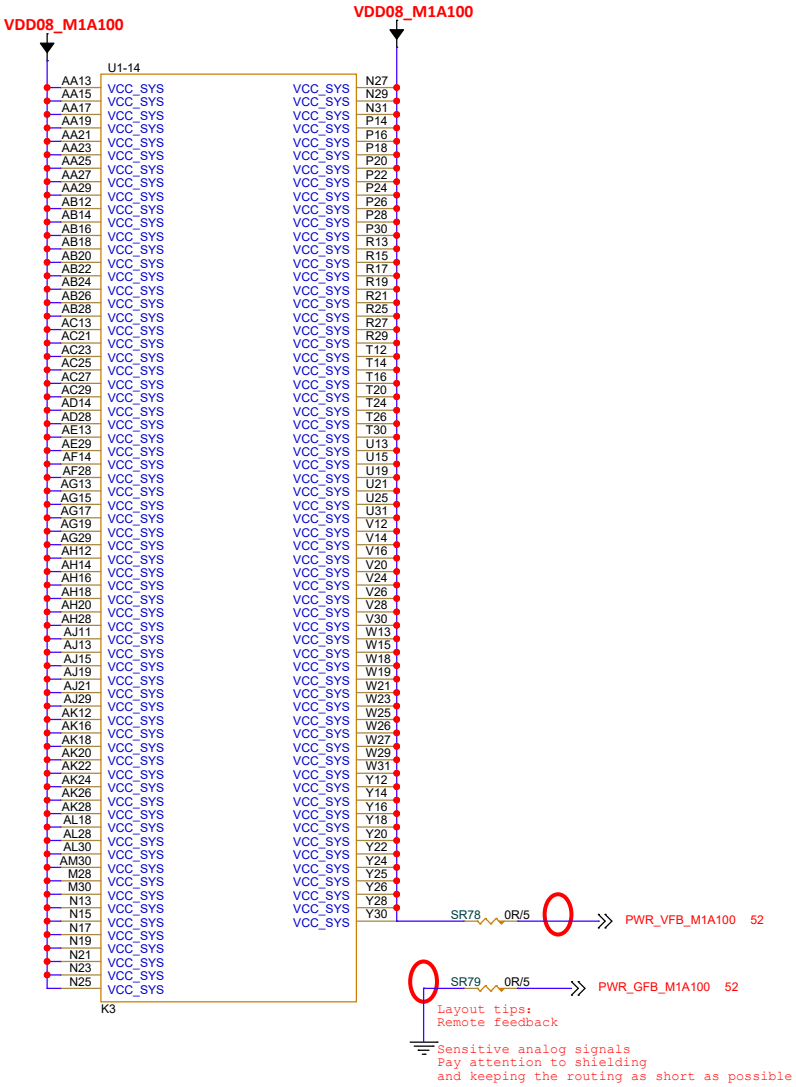
VCC-SYS









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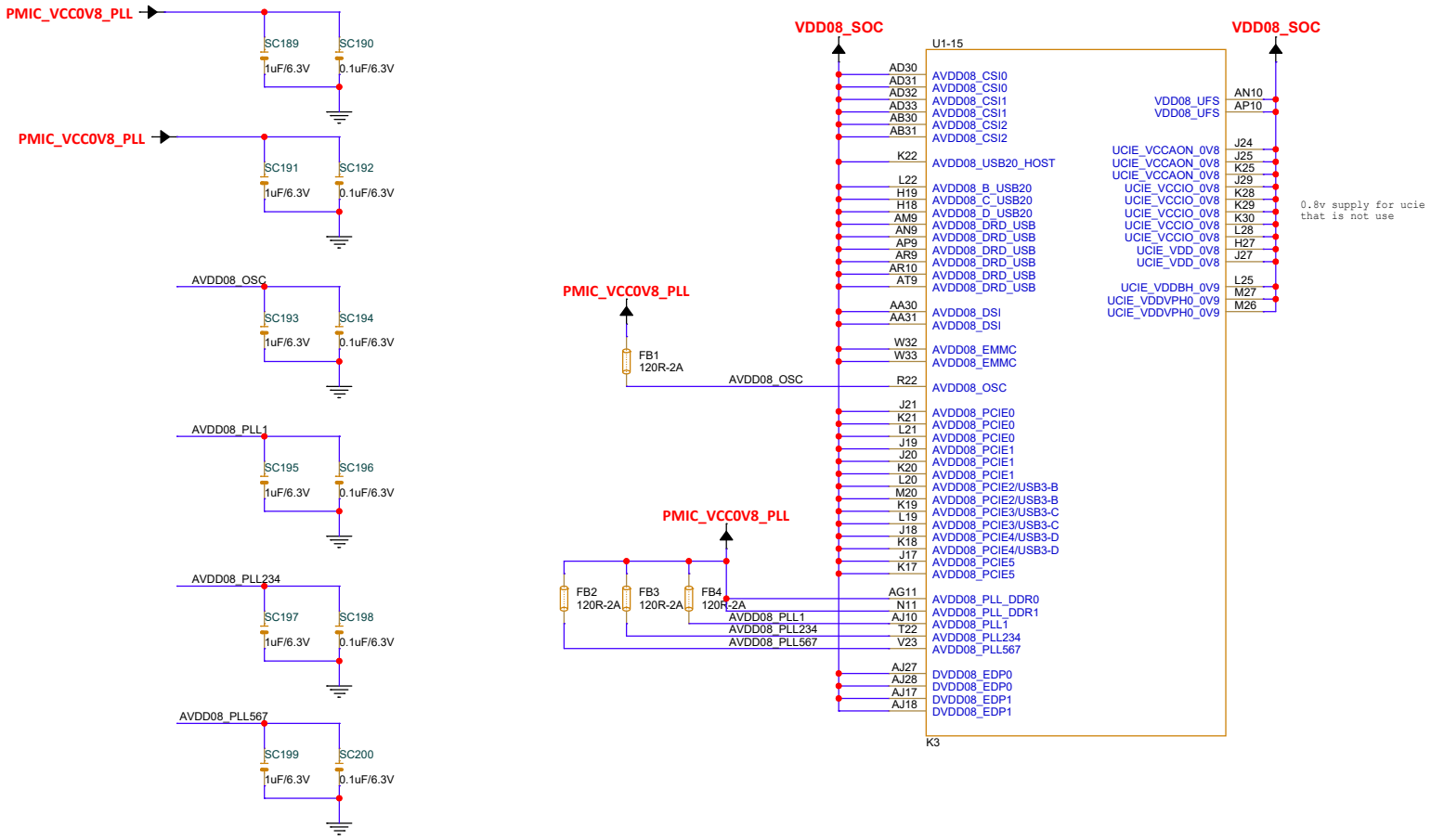
VCC-0V8-PHY



Title	<Title>		
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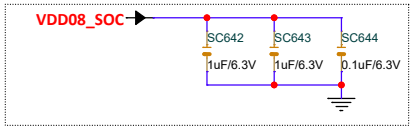
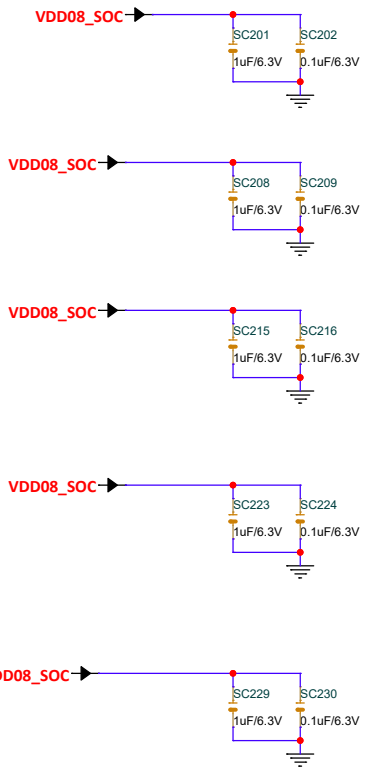
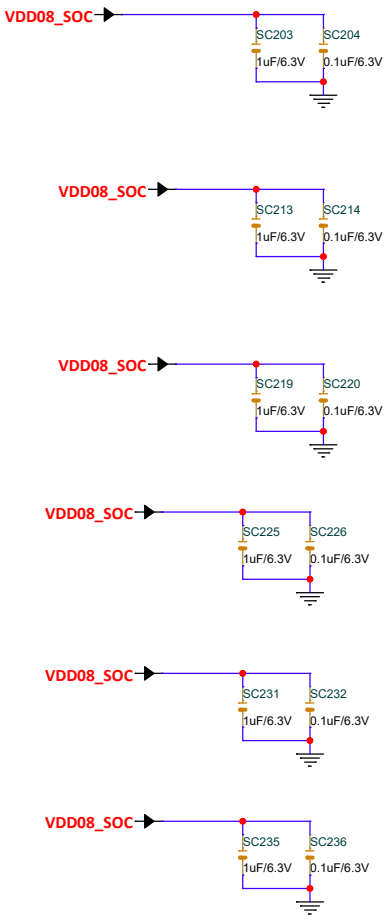
SOC-0V8-PHY CAP



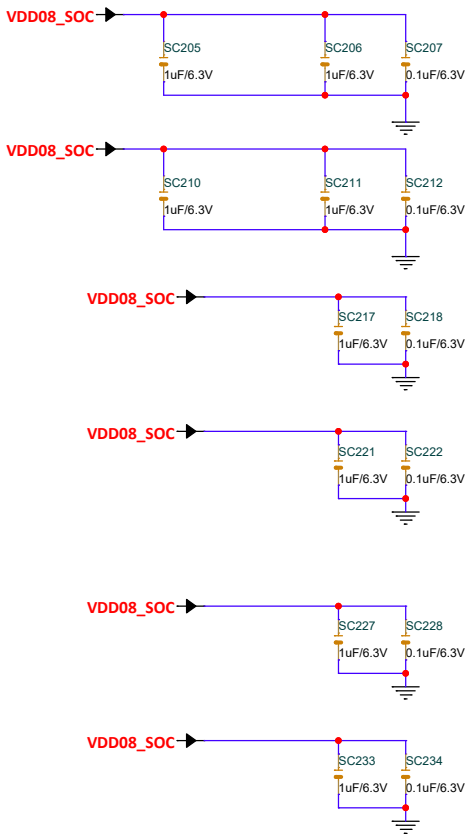
USB20-PHY-CAP



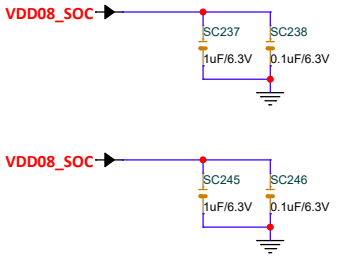
Media PHY-CAP



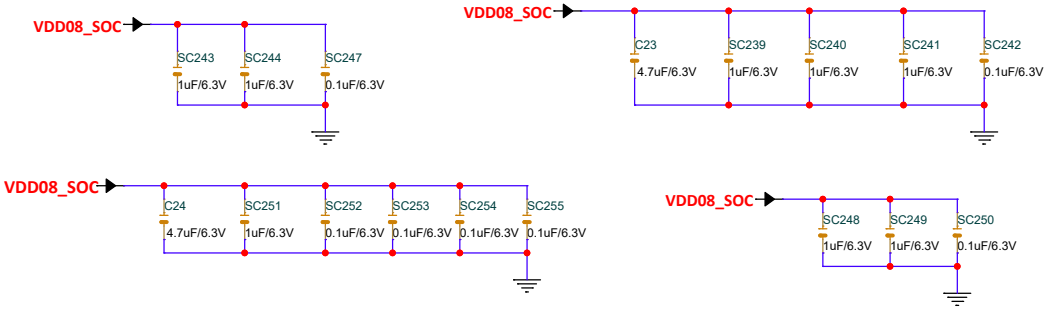
PCIe PHY-CAP



ANA-CAP



UCIe PHY-CAP



Title	<Title>	
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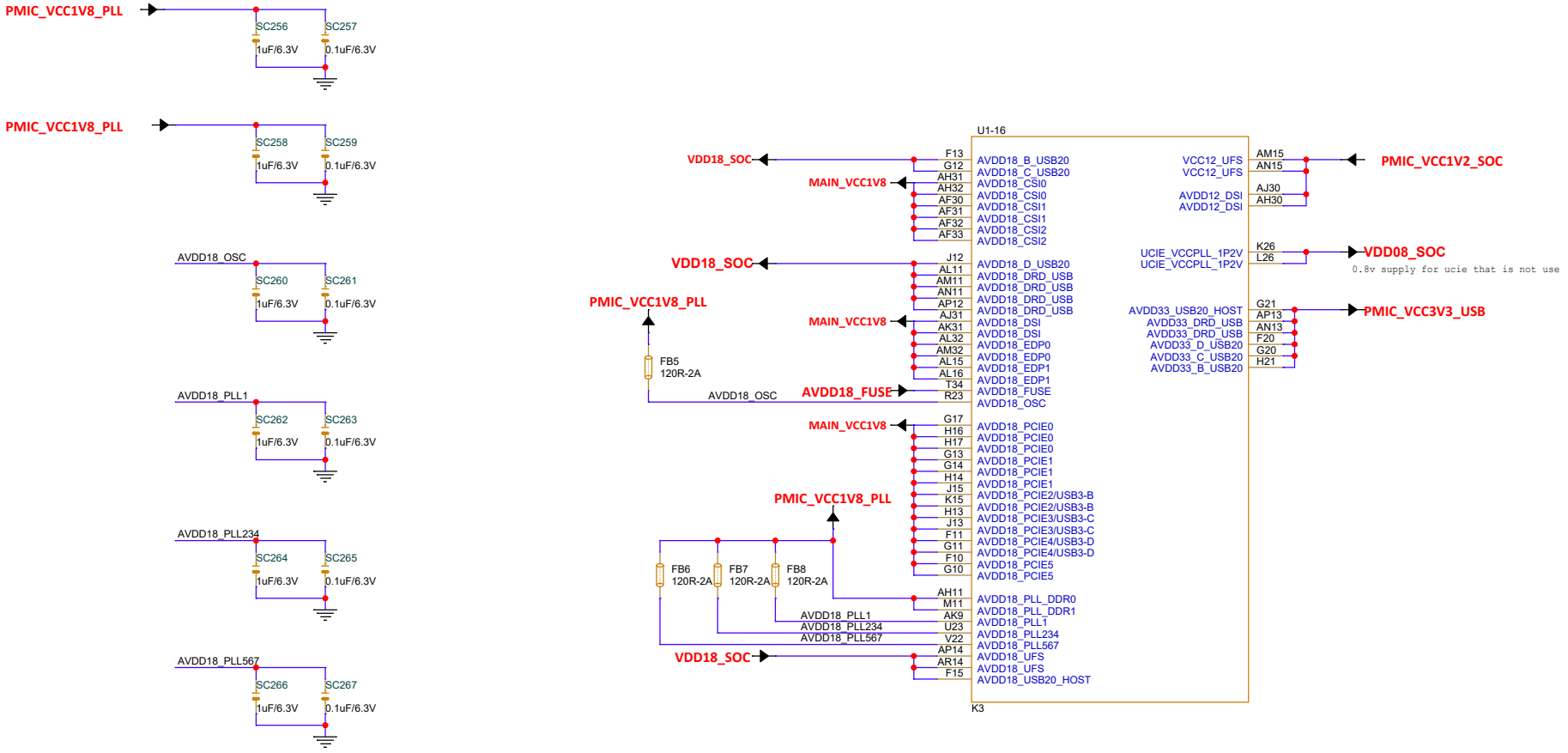
VCC PHY PWR



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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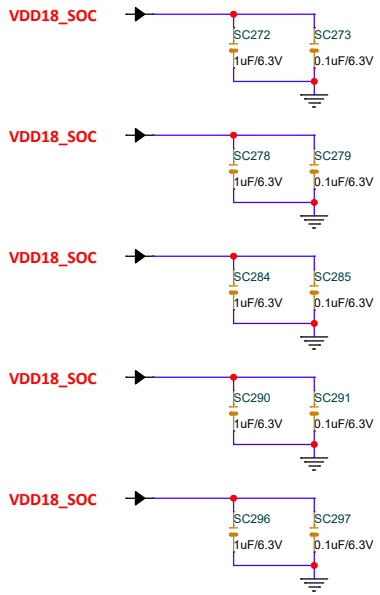
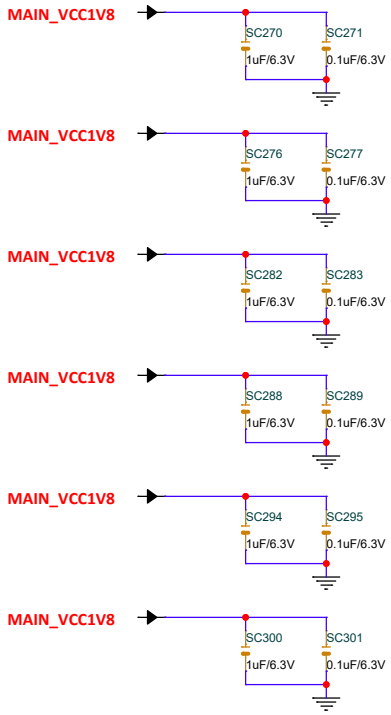
SOC-PWR CAP

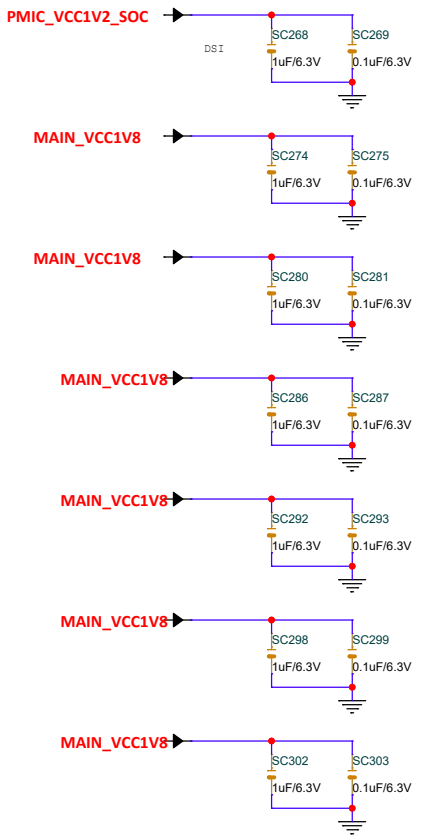
USB20-PHY-1V8



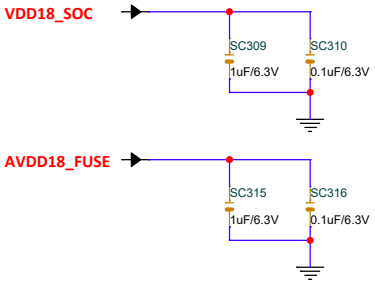
PCIe PHY-CAP



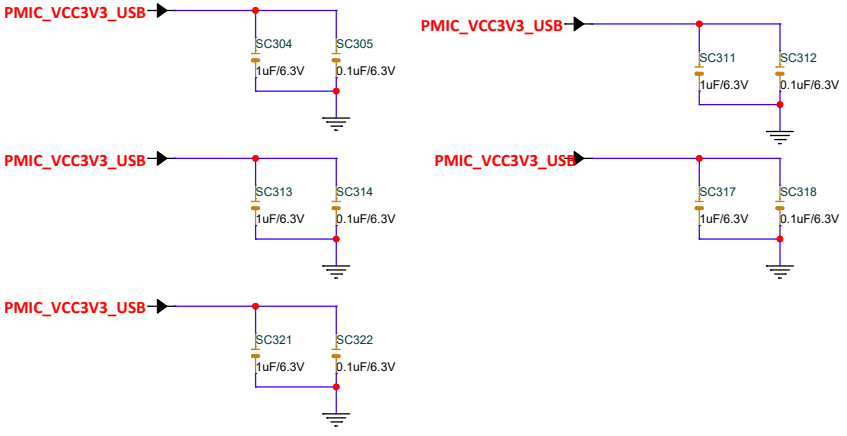
Media PHY-CAP



ANA-CAP



PHY-3V3 1v2



Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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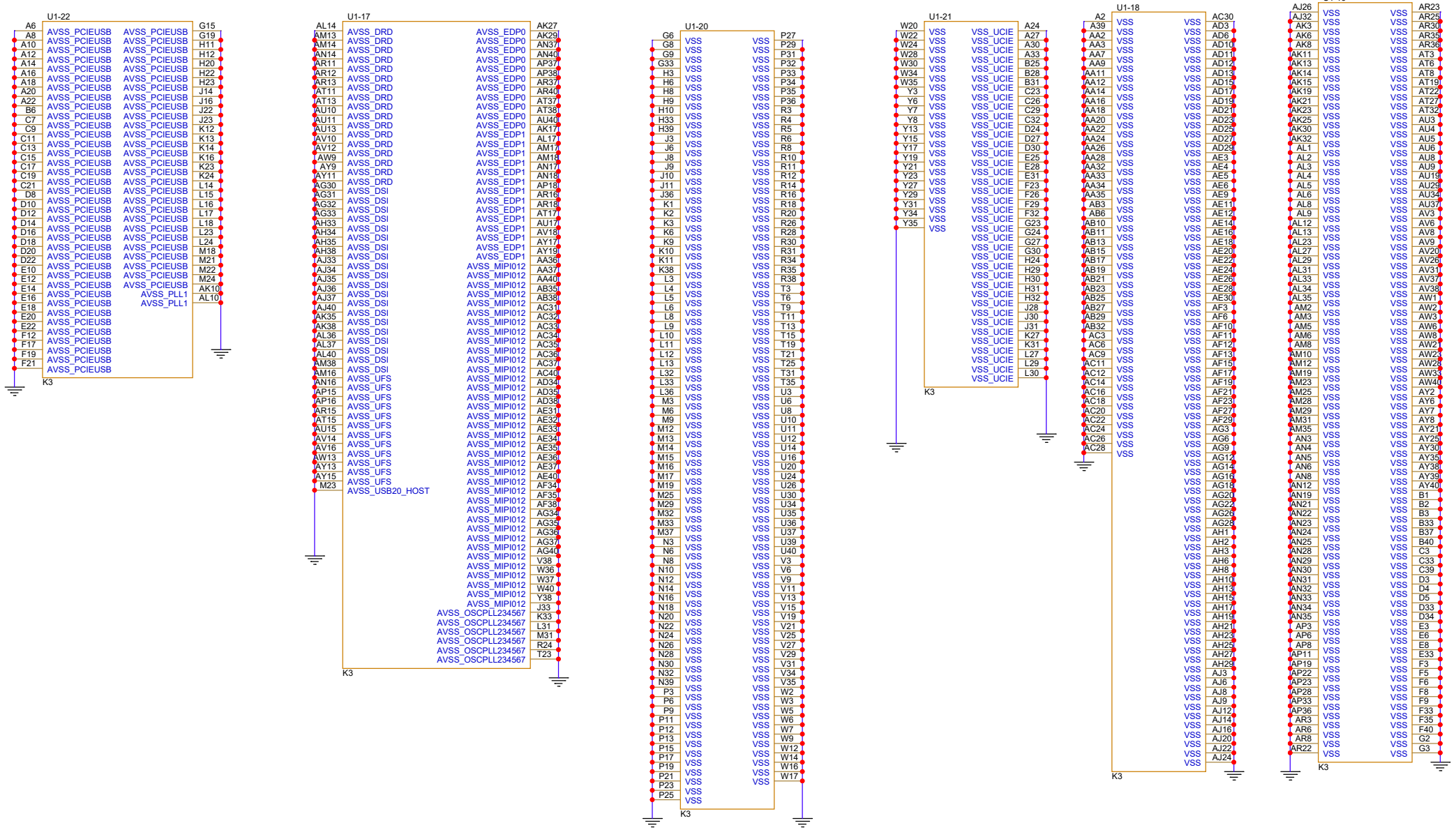

Title	<Title>		
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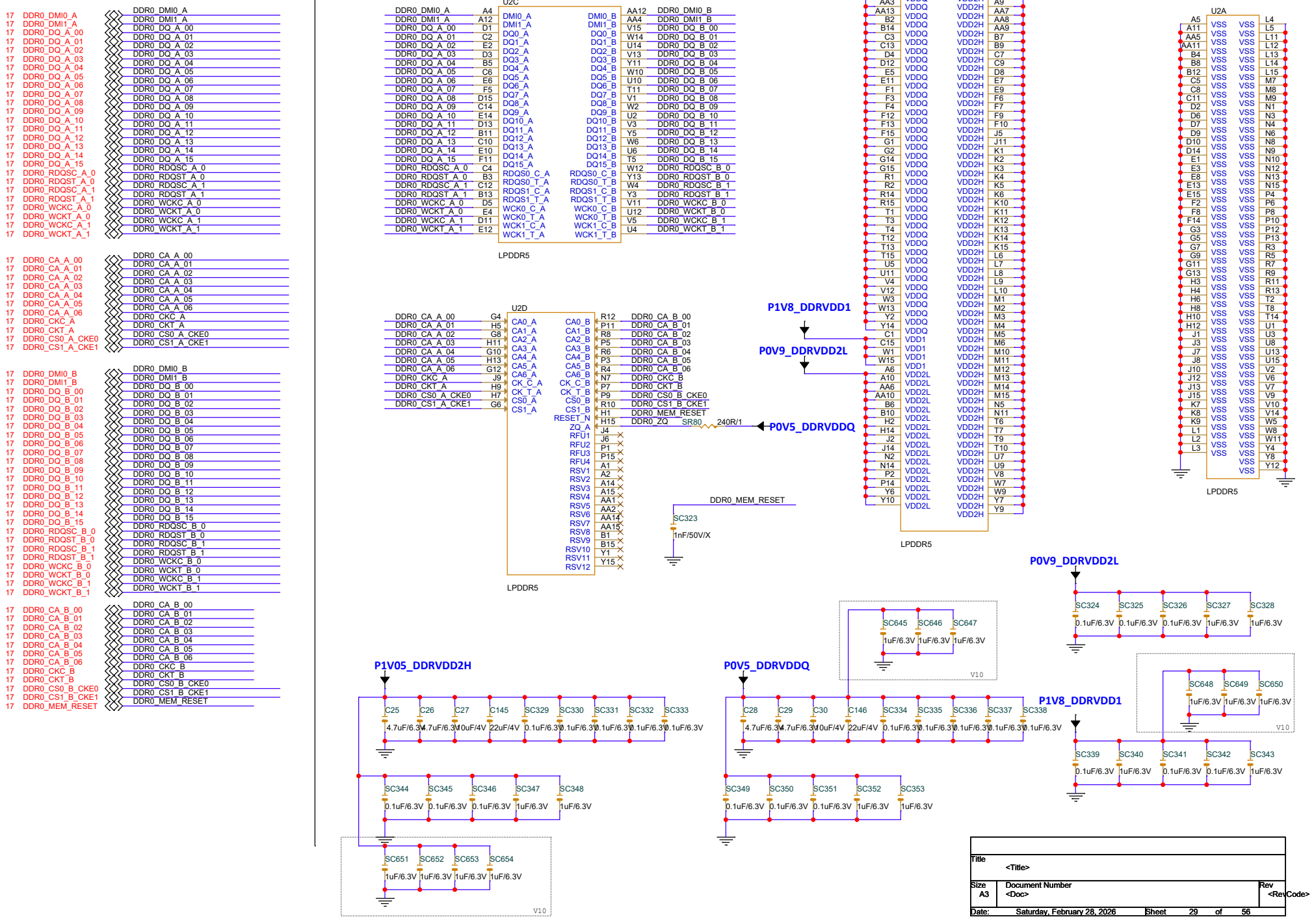
LPDDR5-0



Title	<Title>
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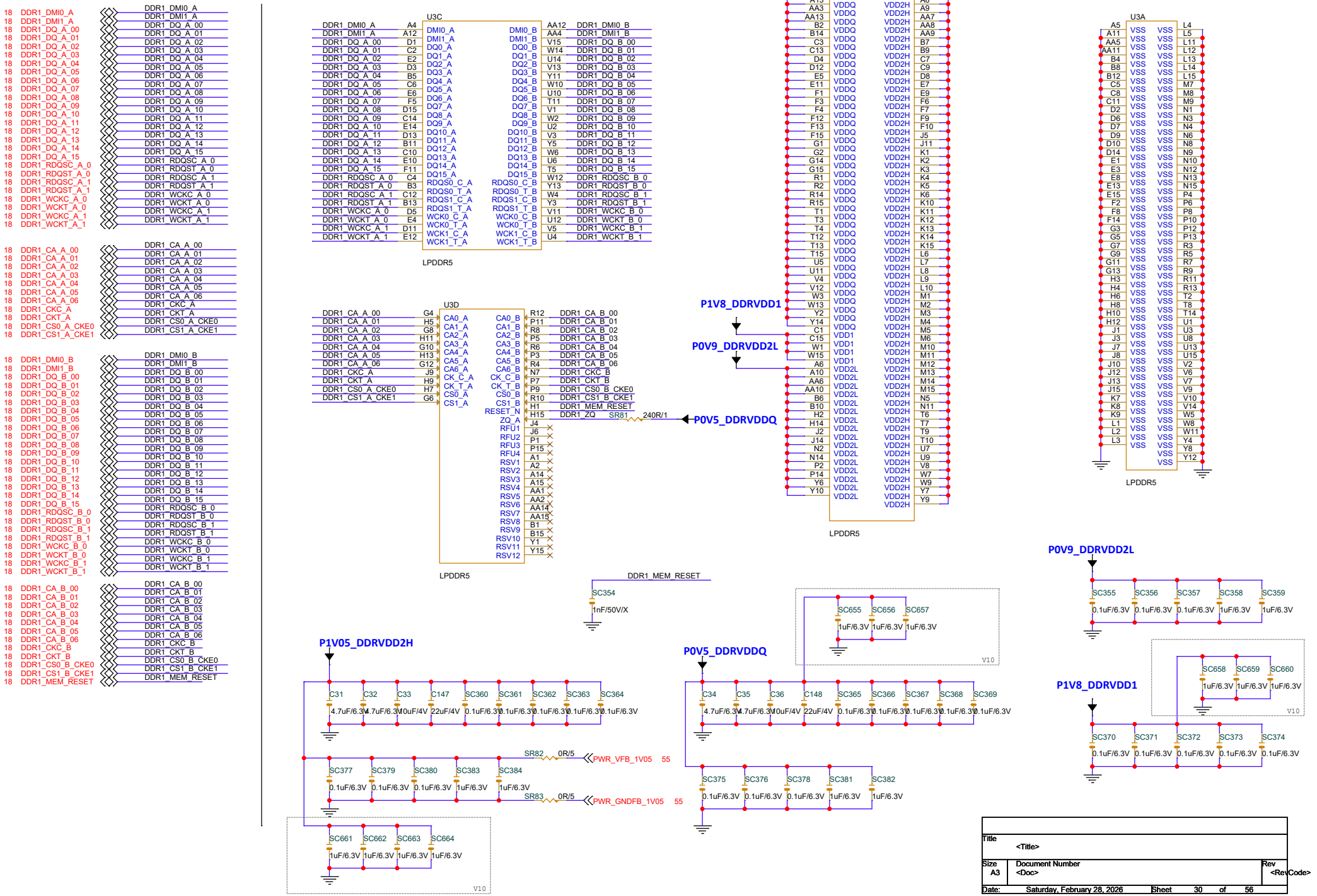
LPDDR5-1



Title	<Title>
Size A3	Document Number <Doc>
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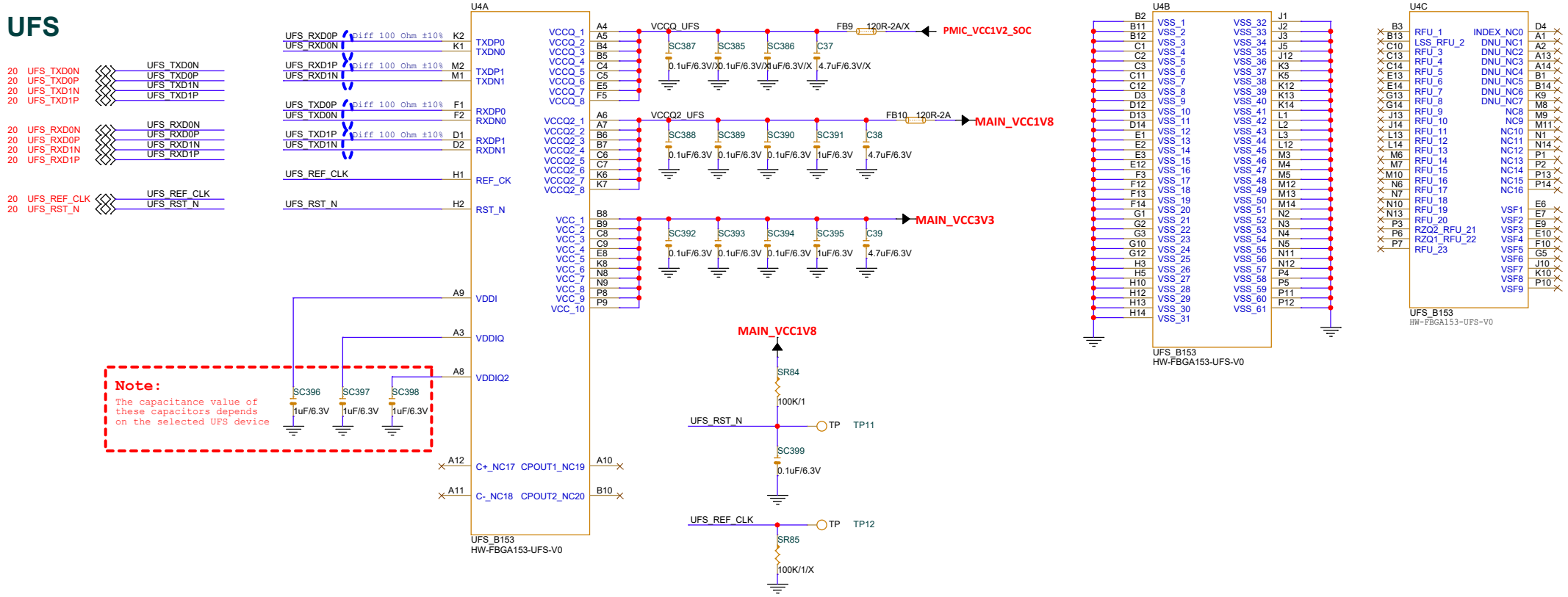
UFS



Supported Particles	VCCQ	VCCQ2	VCC	
UFS2.0	1.2V	1.8V	3.3V	Default UFS device: UFS2.2
UFS2.1	No Connect	1.8V	3.3V	
UFS2.2	No Connect	1.8V	3.3V	
UFS3.0	1.2V	No Connect	2.5V/3.3V	
UFS3.1	1.2V	No Connect	2.5V/3.3V	
Do not support UFS4.0 Device!				

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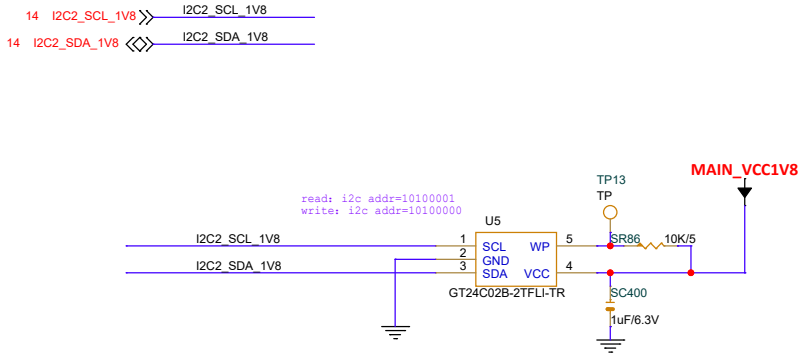
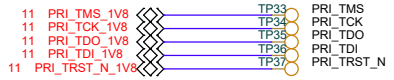
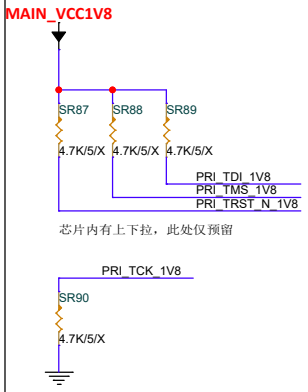
EEPROM

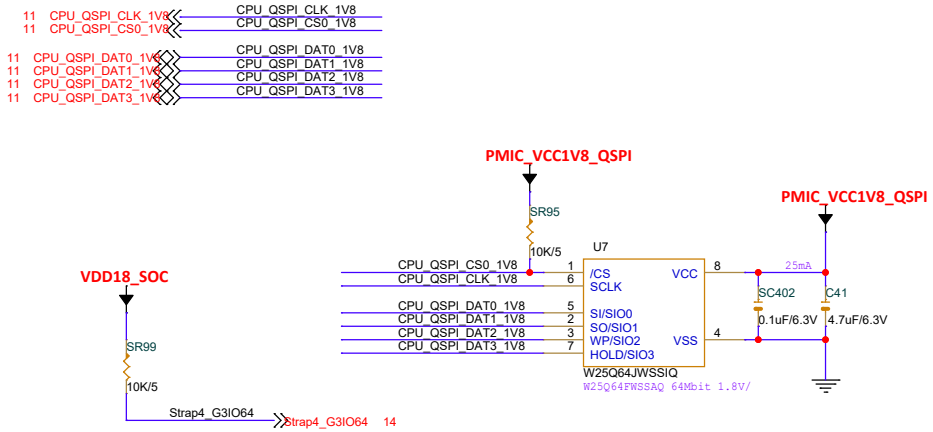


JTAG





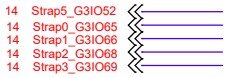
SPI FLASH

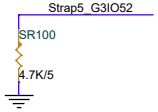


Flash boot voltage(qspi)

GPIO64	Voltage
0	3.3V
1	1.8V

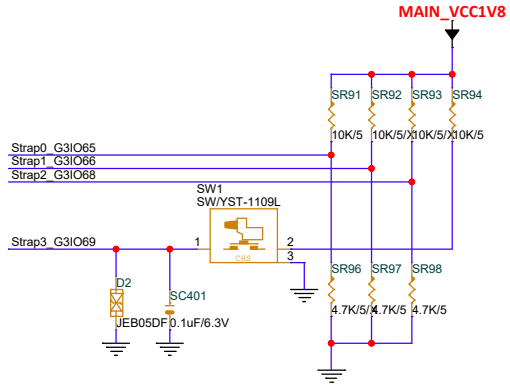
BOOT





DDR Select

GPIO52	Function
0	**LPDDR5**
1	LPDDR4/4x



boot download sel download sel

GPIO69	Function
0	启动
1	下载

GPIO68	Function
0	USB(default)
1	UART

Boot SEL

GPIO66	GPIO65	Function
0	0	TF Card -> EMMC
0	1	**TF Card -> SPI NOR**
1	0	TF Card -> SPI NAND
1	1	TF Card -> UFS

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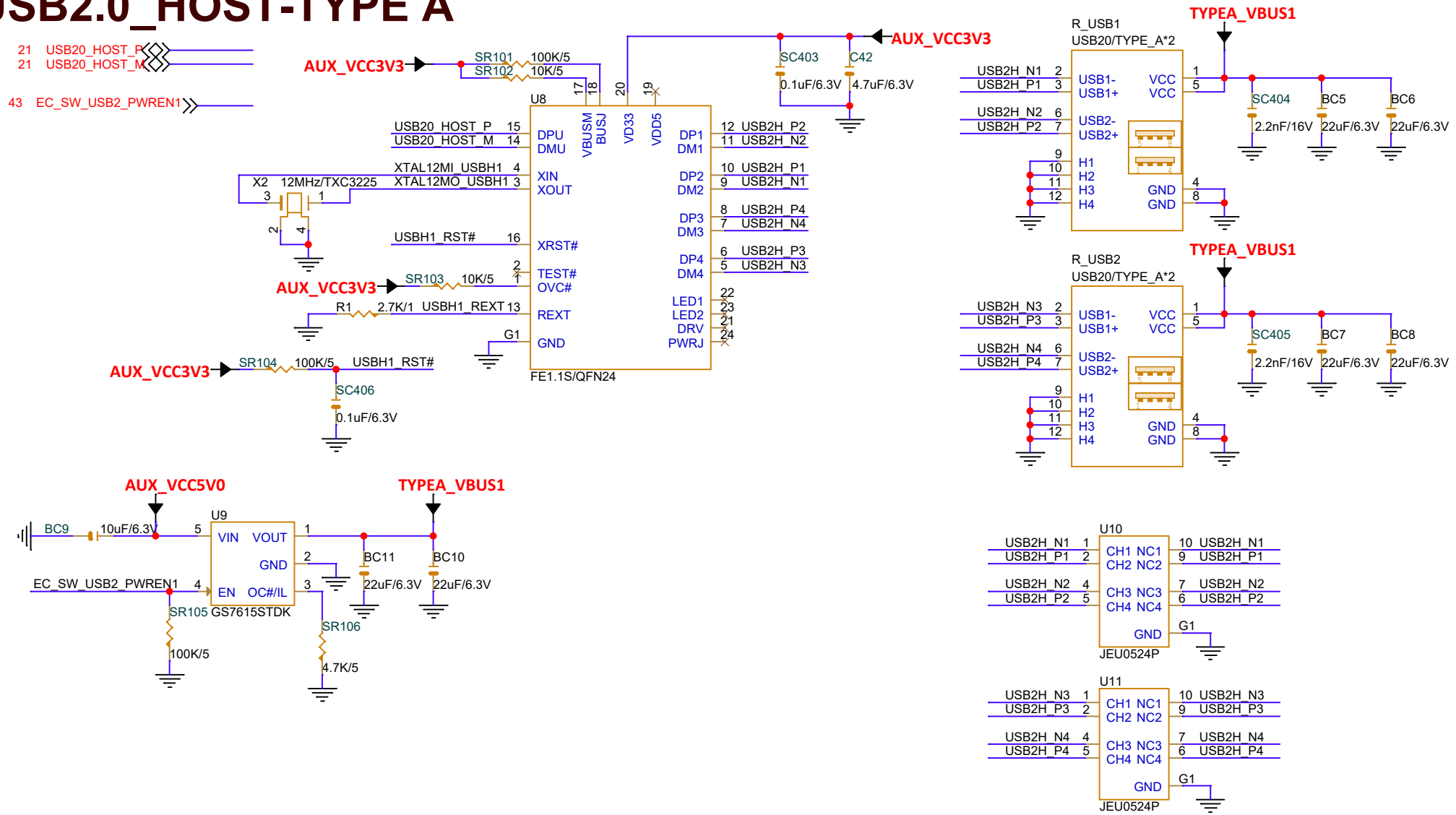
USB2.0_HOST-TYPE A



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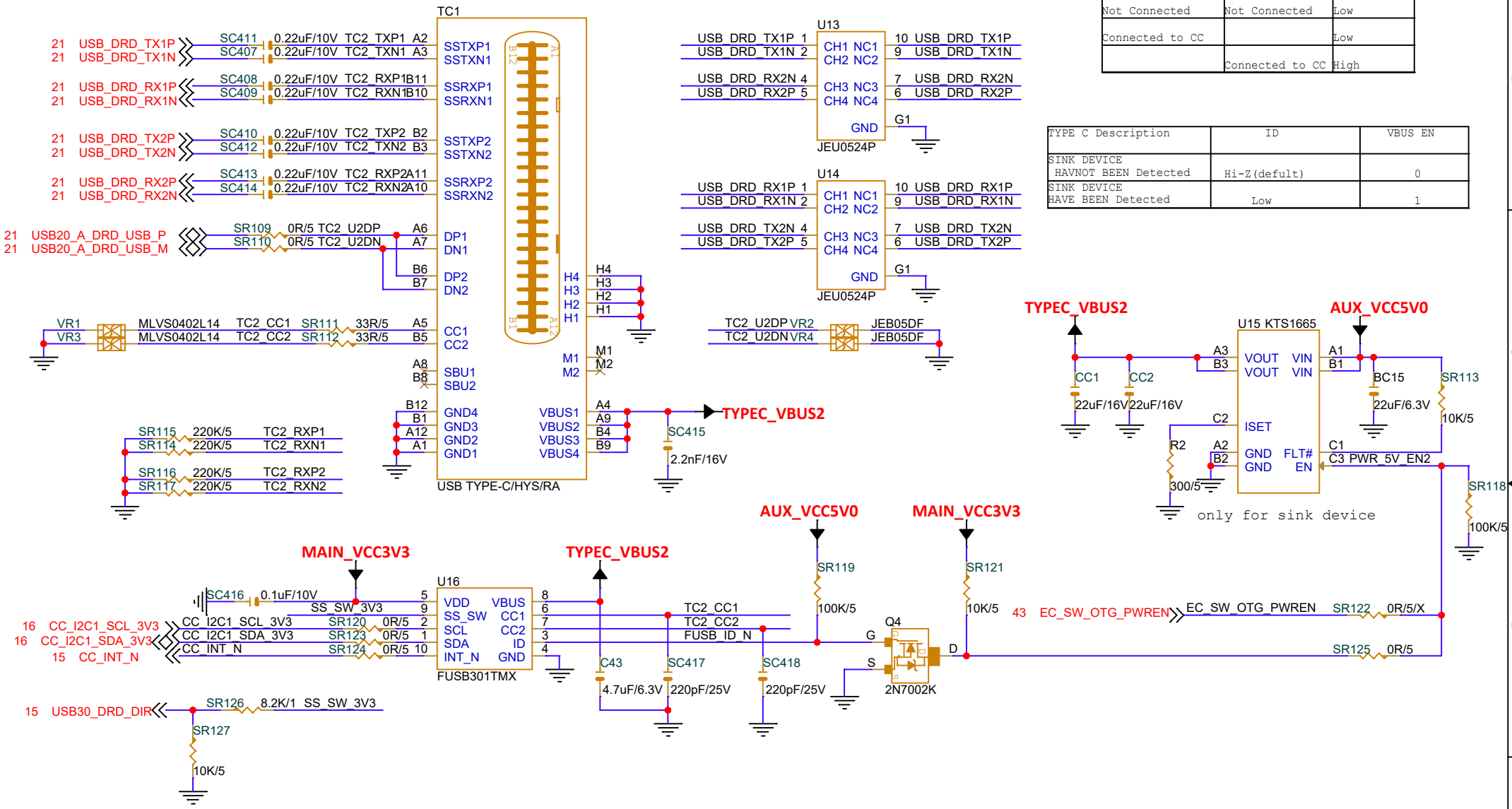
USB3.0-DRD_A Type C

CC1	CC2	SS_SW
Not Connected	Not Connected	Low
Connected to CC		Low
	Connected to CC	High

TYPE C Description	ID	VBUS EN
SINK DEVICE HAVNOT BEEN Detected	Hi-Z(defult)	0
SINK DEVICE HAVE BEEN Detected	Low	1



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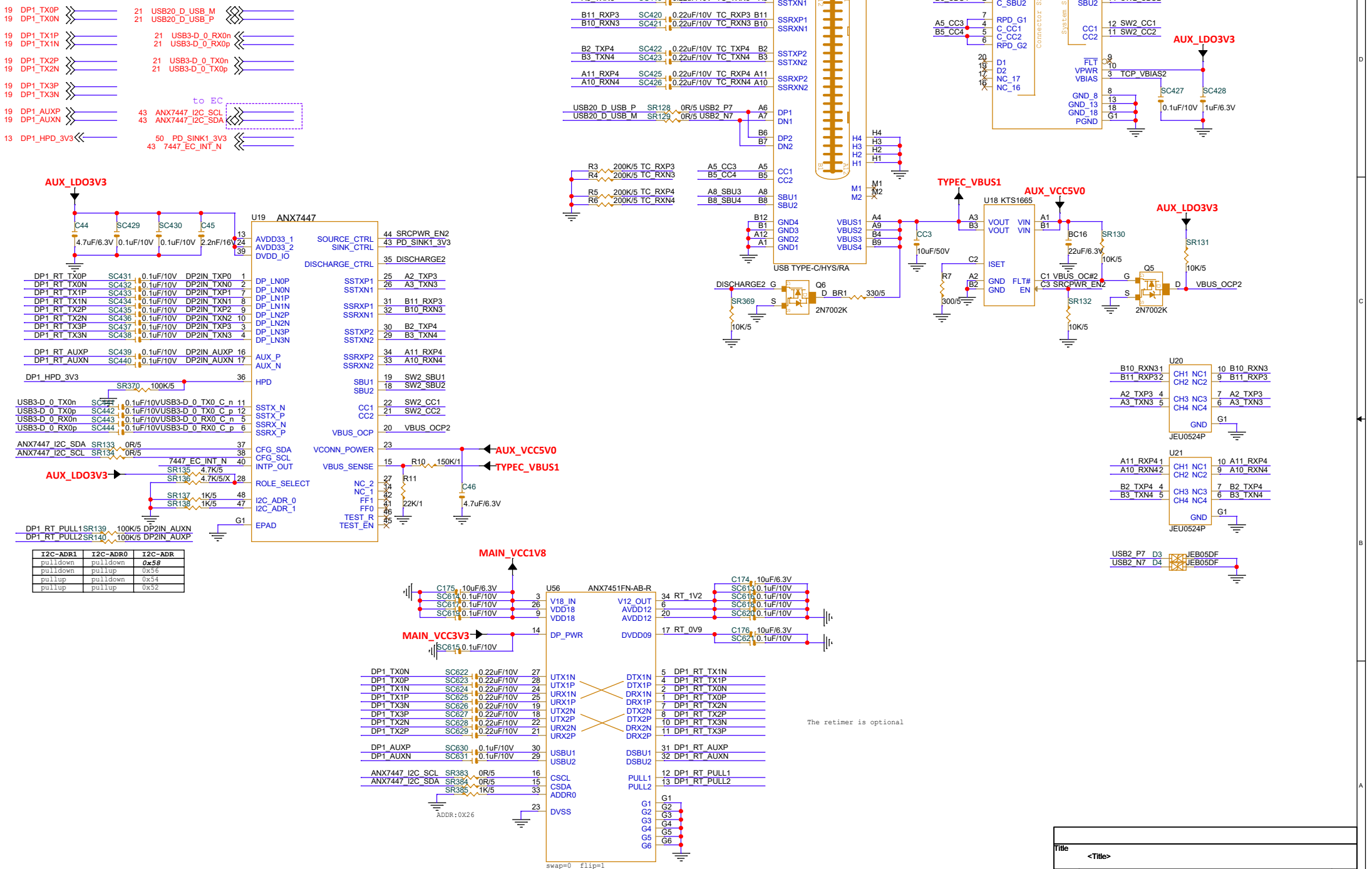
USB3.0 FULL TYPE-C



I2C-ADR1	I2C-ADR0	I2C-ADR
pulldown	pulldown	*0x58*
pulldown	pullup	0x56
pullup	pulldown	0x54
pullup	pullup	0x52

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PCIE 1 MUX 2 : 4

21 PCIe1_TX0p
21 PCIe1_TX0n
21 PCIe1_RX0p
21 PCIe1_RX0n
21 PCIe1_TX1p
21 PCIe1_TX1n
21 PCIe1_RX1p
21 PCIe1_RX1n

37 MUX-A_TX0P
37 MUX-A_TX0N
37 MUX-A_RX0P
37 MUX-A_RX0N
37 MUX-A_TX1P
37 MUX-A_TX1N
37 MUX-A_RX1P
37 MUX-A_RX1N

38 MUX-B_TX0P
38 MUX-B_TX0N
38 MUX-B_RX0P
38 MUX-B_RX0N
38 MUX-B_TX1P
38 MUX-B_TX1N
38 MUX-B_RX1P
38 MUX-B_RX1N

15,37 MUX_SEL33

M-KEY X2 , B-KEY X2

M-KEY X4

MUX_SEL	SW_PORT	PCIE_CONTROLLER
0	A	1
1	B	0

U22 GMA340

AUX_VCC3V3
17 VDD
SC445
0.1uF/10V
3 NC1
12 NC2
SEL:
L:CHB
H:CHC

PCIe1_TX0p 2 A0+
PCIe1_TX0n 1 A0-
PCIe1_RX0p 5 A1+
PCIe1_RX0n 4 A1-
B0+ 15 MUX-A_TX0P
B0- 16 MUX-A_TX0N
B1+ 10 MUX-A_RX0P
B1- 11 MUX-A_RX0N

AUX_VCC3V3 SR141 10K/5 MUX_SEL33 6 SEL
7 /OE
C0+ 13 MUX-B_TX0P
C0- 14 MUX-B_TX0N
C1+ 8 MUX-B_RX0P
C1- 9 MUX-B_RX0N

18 GND
19 EPAD

U26 GMA340

AUX_VCC3V3
17 VDD
SC446
0.1uF/10V
3 NC1
12 NC2
SEL:
L:CHB
H:CHC

PCIe1_TX1p 2 A0+
PCIe1_TX1n 1 A0-
PCIe1_RX1p 5 A1+
PCIe1_RX1n 4 A1-
B0+ 15 MUX-A_TX1P
B0- 16 MUX-A_TX1N
B1+ 10 MUX-A_RX1P
B1- 11 MUX-A_RX1N

MUX_SEL33 6 SEL
7 /OE
C0+ 13 MUX-B_TX1P
C0- 14 MUX-B_TX1N
C1+ 8 MUX-B_RX1P
C1- 9 MUX-B_RX1N

18 GND
19 EPAD

U23

MUX-A_TX0P 1 CH1 NC1 10 MUX-A_TX0P
MUX-A_TX0N 2 CH2 NC2 9 MUX-A_TX0N
MUX-A_RX0P 4 CH3 NC3 7 MUX-A_RX0P
MUX-A_RX0N 5 CH4 NC4 6 MUX-A_RX0N
GND G1
JEU0524P/X

U24

MUX-B_TX0P 1 CH1 NC1 10 MUX-B_TX0P
MUX-B_TX0N 2 CH2 NC2 9 MUX-B_TX0N
MUX-B_RX0P 4 CH3 NC3 7 MUX-B_RX0P
MUX-B_RX0N 5 CH4 NC4 6 MUX-B_RX0N
GND G1
JEU0524P/X

U25

MUX-A_TX1P 1 CH1 NC1 10 MUX-A_TX1P
MUX-A_TX1N 2 CH2 NC2 9 MUX-A_TX1N
MUX-A_RX1P 4 CH3 NC3 7 MUX-A_RX1P
MUX-A_RX1N 5 CH4 NC4 6 MUX-A_RX1N
GND G1
JEU0524P/X

U27

MUX-B_TX1P 1 CH1 NC1 10 MUX-B_TX1P
MUX-B_TX1N 2 CH2 NC2 9 MUX-B_TX1N
MUX-B_RX1P 4 CH3 NC3 7 MUX-B_RX1P
MUX-B_RX1N 5 CH4 NC4 6 MUX-B_RX1N
GND G1
JEU0524P/X

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PCIE B M.2 KEY B x2

36 MUX-A_TX0P
36 MUX-A_TX0N
36 MUX-A_RX0P
36 MUX-A_RX0N
36 MUX-A_TX1P
36 MUX-A_TX1N
36 MUX-A_RX1P
36 MUX-A_RX1N
21 USB20_B_USB_M
21 USB20_B_USB_P
12 Module_Turn_ON_1V8
12 WWAN_Reset#_1V8
15 CPU_W_DISABLE#1
15,36 MUX_SEL33

15 PCIe1_PERSTn
43 PCIe1_WAKEn
15 PCIe1_CLKREQn
21 PCIe1_REFCLK_p
21 PCIe1_REFCLK_n

SIM1
CLK_UIM1 SR143 22R/5
RST_UIM1 SR145 22R/5
PWR_UIM1
RSV4 RSV8 DAT VPP GND CLK REST VCC
C4 C3 C2 C1 C8 C7 C6 C5
SR144 22R/5 DAT_UIM1
SR142 10K/5 PWR_UIM1
MICROSIM/LOCK
G1 G2 G3 G4

DAT_UIM1 D5 JEB05DF
CLK_UIM1 D6 JEB05DF
RST_UIM1 D7 JEB05DF
PWR_UIM1 SC447 0.1uF/10V

DAT_UIM1 C47 33pF/50V
CLK_UIM1 C48 33pF/50V
RST_UIM1 C49 33pF/50V

MAIN_VCC3V3
BC17 22uF/6.3V
SC448 10nF/10V

M2_KBM1
TOP ROW
1 CFG3/PSNT#
3 GND3
5 GND5/M_PERN3
7 USB_D+/M_PERP3
9 USB_D-/M_GND9
11 GND11/M_PETN3
13 BK13/M_PETP3
15 BK15/M_GND15
17 BK17/M_PERN2
19 BK19/M_PERP2
21 CFG0/OC_SSD
23 GP11/WOWWAN#/M_PETN2
25 DPR/M_PETP2
27 GND27
29 PERN1/U3RXN
31 PERP1/U3RXP
33 GND33
35 PETN1/U3TXN
37 PETP1/U3TXP
39 GND39
41 SATA_HRXP/PERN0
43 SATA_HRXN/PERP0
45 GND45
47 SATA_HTXN/PETN0
49 SATA_HTXP/PETP0
51 GND51
53 REFCLKN
55 REFCLKP
57 GND57
59 ANTCTL0/MK59
61 ANTCTL1/MK61
63 ANTCTL2/MK63
65 ANTCTL3/MK65
67 WWAN1V8_RST#
69 OC_PE/GND_SATA
71 GND71
73 GND73
75 IND_USB3/GND_OTHER
2 3.3Vaux_2
4 3.3Vaux_4
6 FC_PWROFF#
8 WWAN_DIS#
10 GP9/DSS#(OD)
12 BK12/M_3V3
14 BK14/M_3V3
16 BK16/M_3V3
18 BK18_M3V3
B key
20 GP5
22 GP6
24 GP7
26 GP10/GPS_DIS#
28 GP8/GPS_PWR1V8
30 UIM_RST
32 UIM_CLK
34 UIM_DAT
36 UIM_PWR
38 DEVSLP(I)(0/3.3V)
40 GP0
42 GP1
44 GP2
46 GP3
48 GP4
50 PERST#
52 CLKREQ#
54 PEWAKE#
56 SDA
58 SCL
M key
60 COEX3/MK60
62 COEX2/MK62
64 COEX1/MK64
66 SIM_DET/MK66
68 SUSCLK32K
70 3.3Vaux_70
72 3.3Vaux_72
74 3.3Vaux_74
MT1
MT2
BOTTOM ROW
M.2/KEY-B/8.5MM

D8 JEB05DF USB20_B_USB_P
D9 JEB05DF USB20_B_USB_M

CPU_W_DISABLE#1
SR146 22R/5 Module_Turn_ON_1V8
SC449 0.1uF/10V

W_DISABLE#1 飞行模式控制，模块内上拉1.8V

1. 请确保 VCC 电压稳定后再拉高
FULL CARD POWER_OFF#引脚，建议时间间隔不少于 30 ms。2.
在模块开机之后，RESET#会自动拉高。在开机过程中，请勿下拉 RESET#。

MUX_SEL33

MUX-A_RX1N SR147 0R/5 MUX-A_RX1_N
MUX-A_RX1P SR148 0R/5 MUX-A_RX1_P
MUX-A_TX1N SC450 0.22uF/10V MUX-A_TX1_N
MUX-A_TX1P SC451 0.22uF/10V MUX-A_TX1_P
MUX-A_RX0N SR149 0R/5 MUX-A_RX0_N
MUX-A_RX0P SR150 0R/5 MUX-A_RX0_P
MUX-A_TX0N SC452 0.22uF/10V MUX-A_TX0_N
MUX-A_TX0P SC453 0.22uF/10V MUX-A_TX0_P
PCIe1_REFCLK_n
PCIe1_REFCLK_p

RST_UIM1
CLK_UIM1
DAT_UIM1
PWR_UIM1
PCIe1_3V3_PERSTn
PCIe1_CLKREQn
PCIe1_WAKEn

WWAN_Reset#_1V8

注：4G Module软件关机过程中，建议先拉低RESET#
至少100ms后再拉低WWAN_Turn_ON_1V8，否则直接
拉低WWAN_Turn_ON_1V8模块将强制关机，这种关机
方式可能会损坏模块内部存储芯片的数据。

MAIN_VCC3V3
SR428 10K/5
SR429 10K/5
PCIe1_3V3_PERSTn
PCIe1_PERSTn
Q23 PJT7828
SR430 100K/5
V10

MPH1
MPH/6.5MM

BC18 22uF/6.3V
SC454 0.1uF/10V

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PCIE_A&B M.2 KEY M x4

21 PCIe0_REFCLK_P
21 PCIe0_REFCLK_n

21 PCIe0_TX0p
21 PCIe0_TX0n

21 PCIe0_RX0p
21 PCIe0_RX0n

21 PCIe0_TX1p
21 PCIe0_TX1n

21 PCIe0_RX1p
21 PCIe0_RX1n

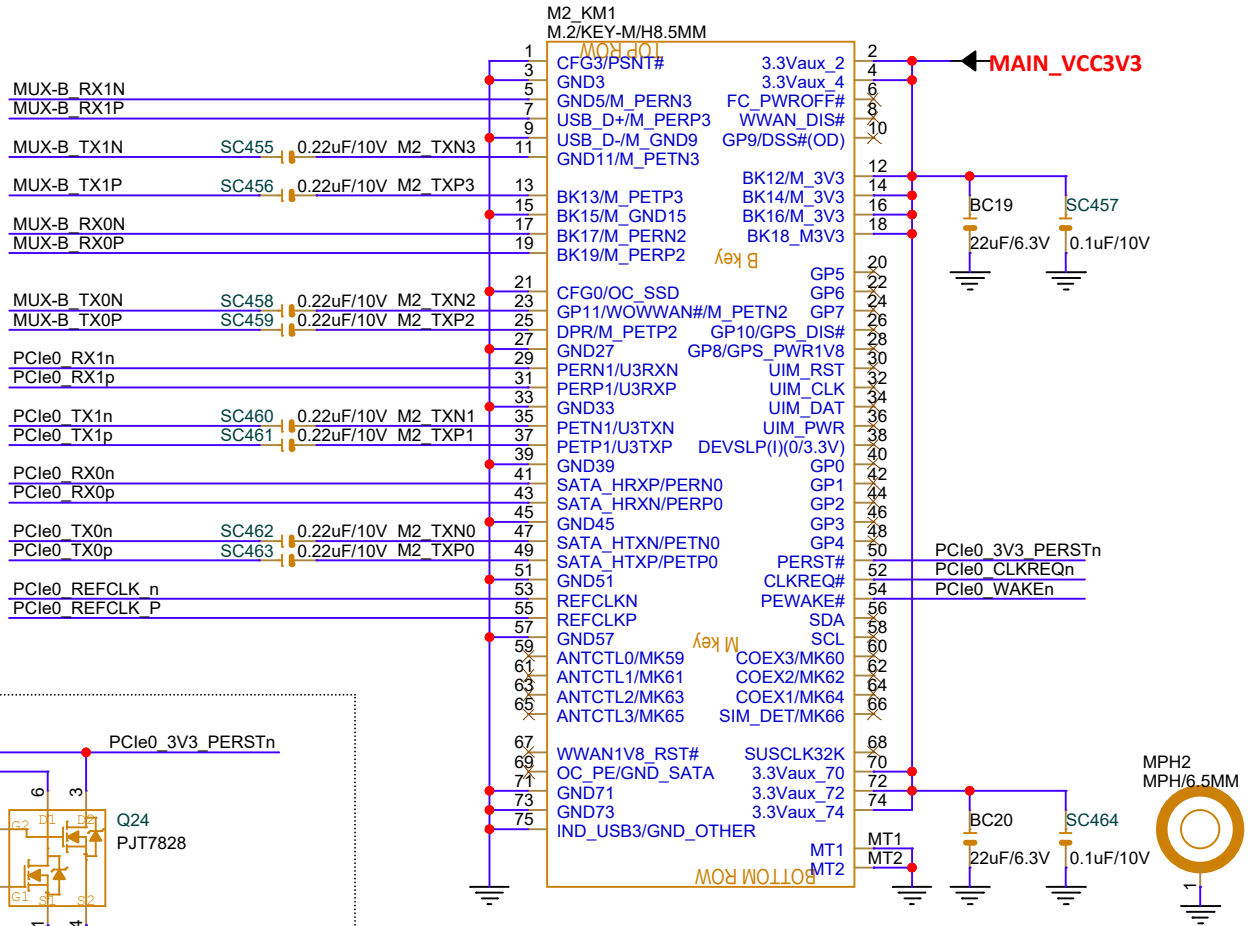
15 PCIe0_PERSTn
43 PCIe0_WAKEn
15 PCIe0_CLKREQn

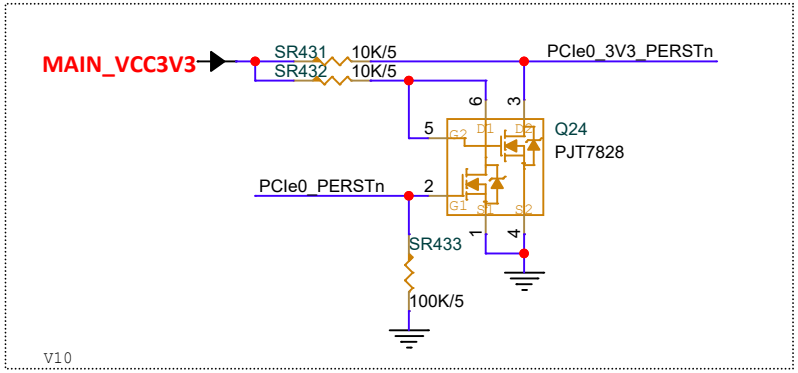
36 MUX-B_TX0P
36 MUX-B_TX0N

36 MUX-B_RX0P
36 MUX-B_RX0N

36 MUX-B_TX1P
36 MUX-B_TX1N

36 MUX-B_RX1P
36 MUX-B_RX1N





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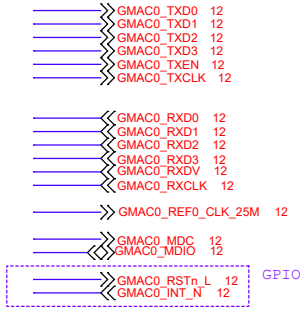
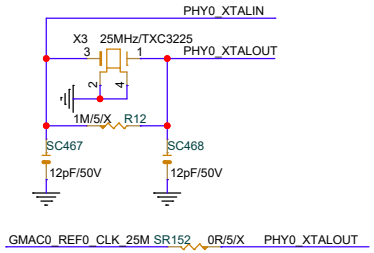
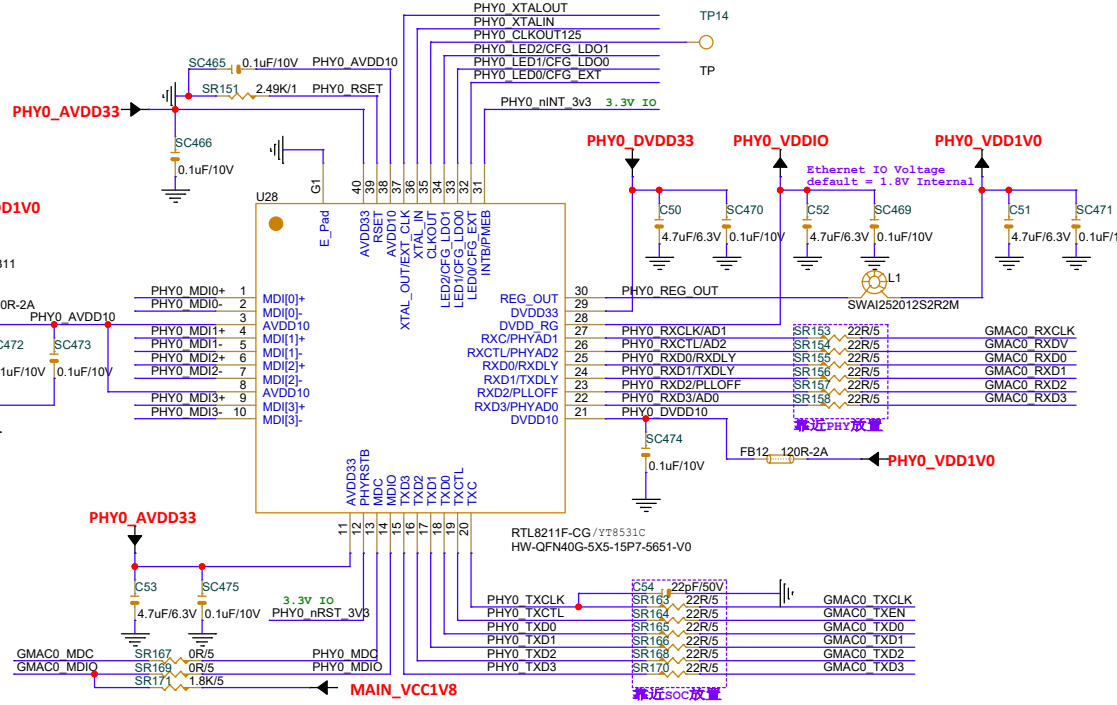
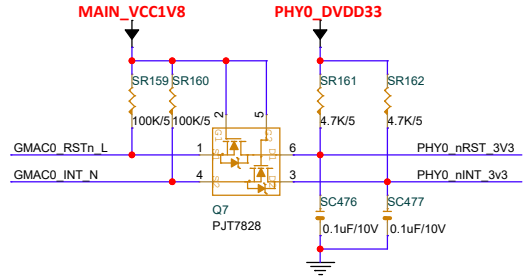
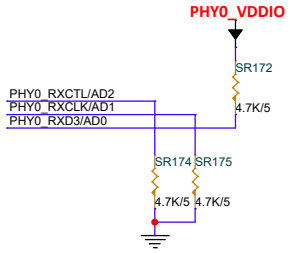
GMAC Ethernet0



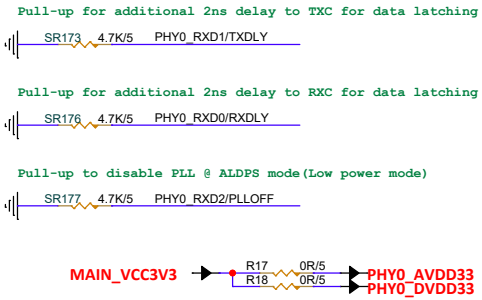


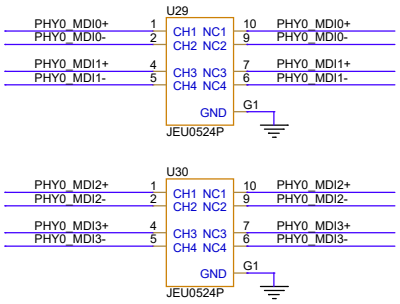


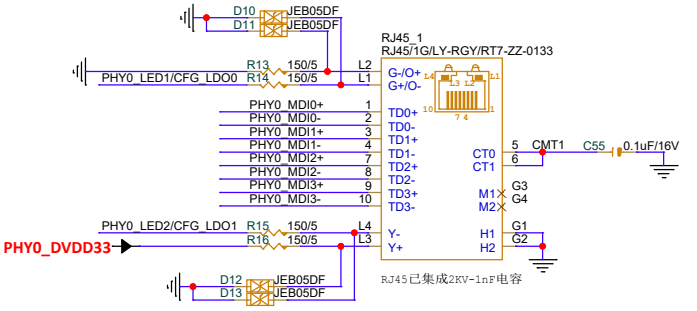


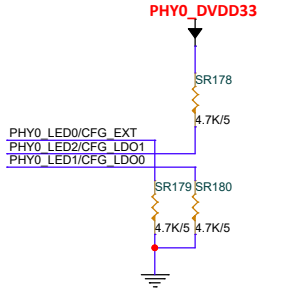


PHY Address	PHYAD[2:0]
1	001









RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(default)	0	10
Internal 1.5V	0	11

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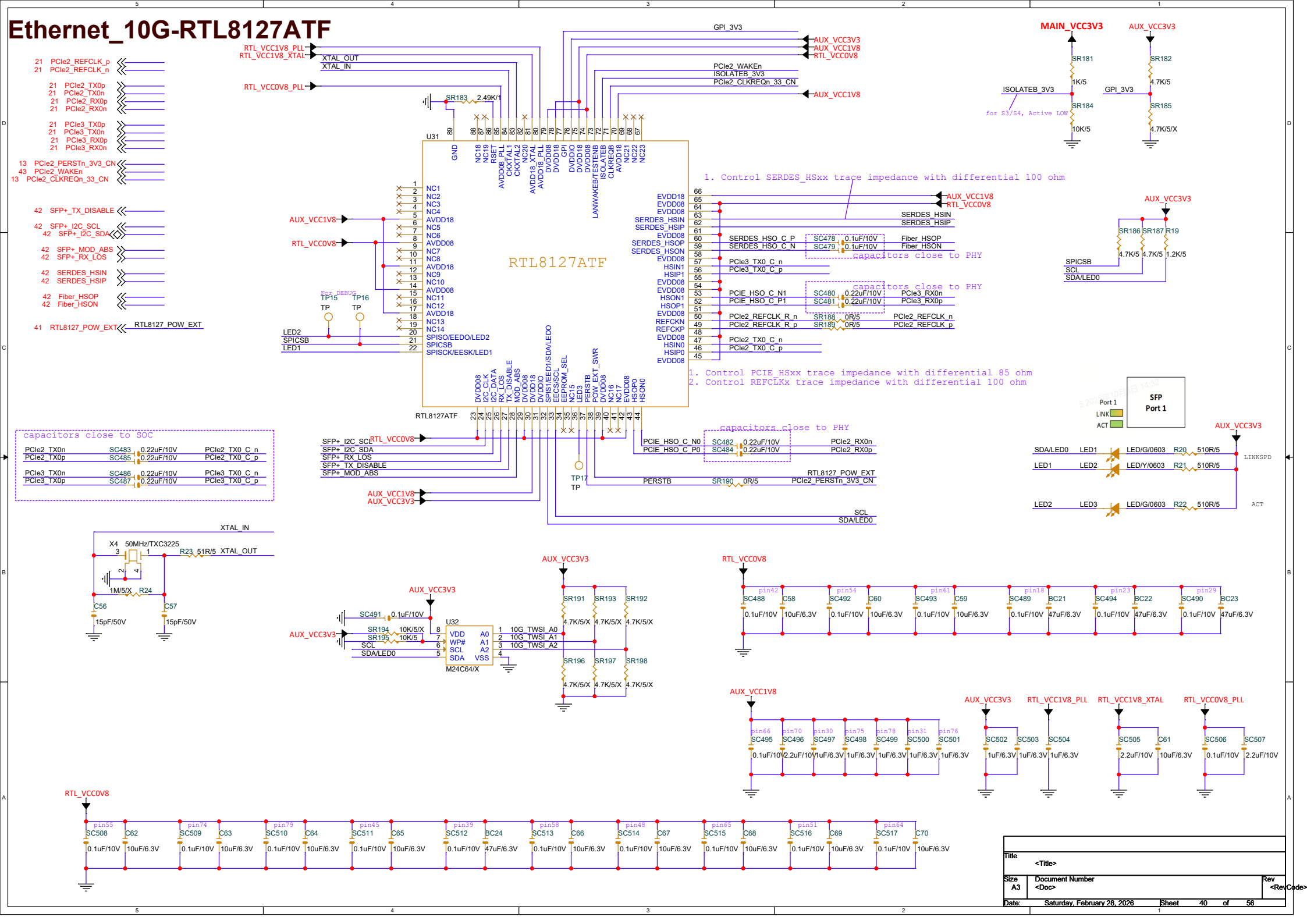
Ethernet_10G-RTL8127ATF



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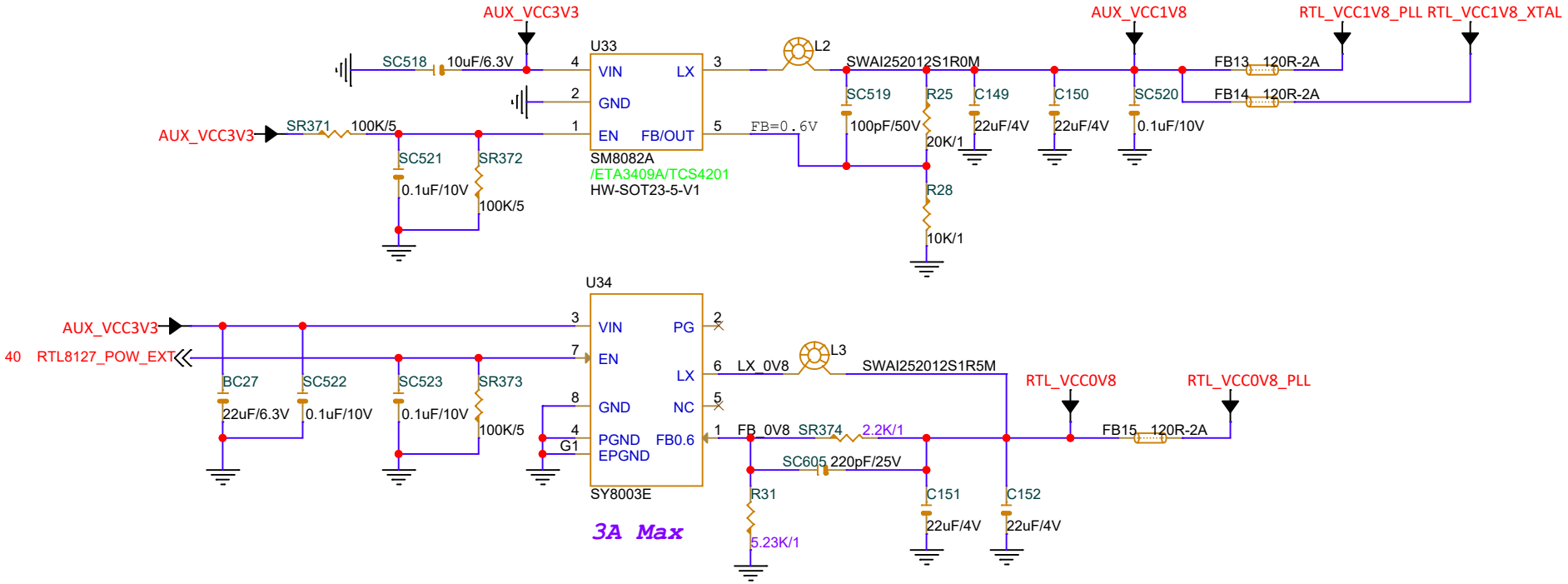
Ethernet_10G-POWER



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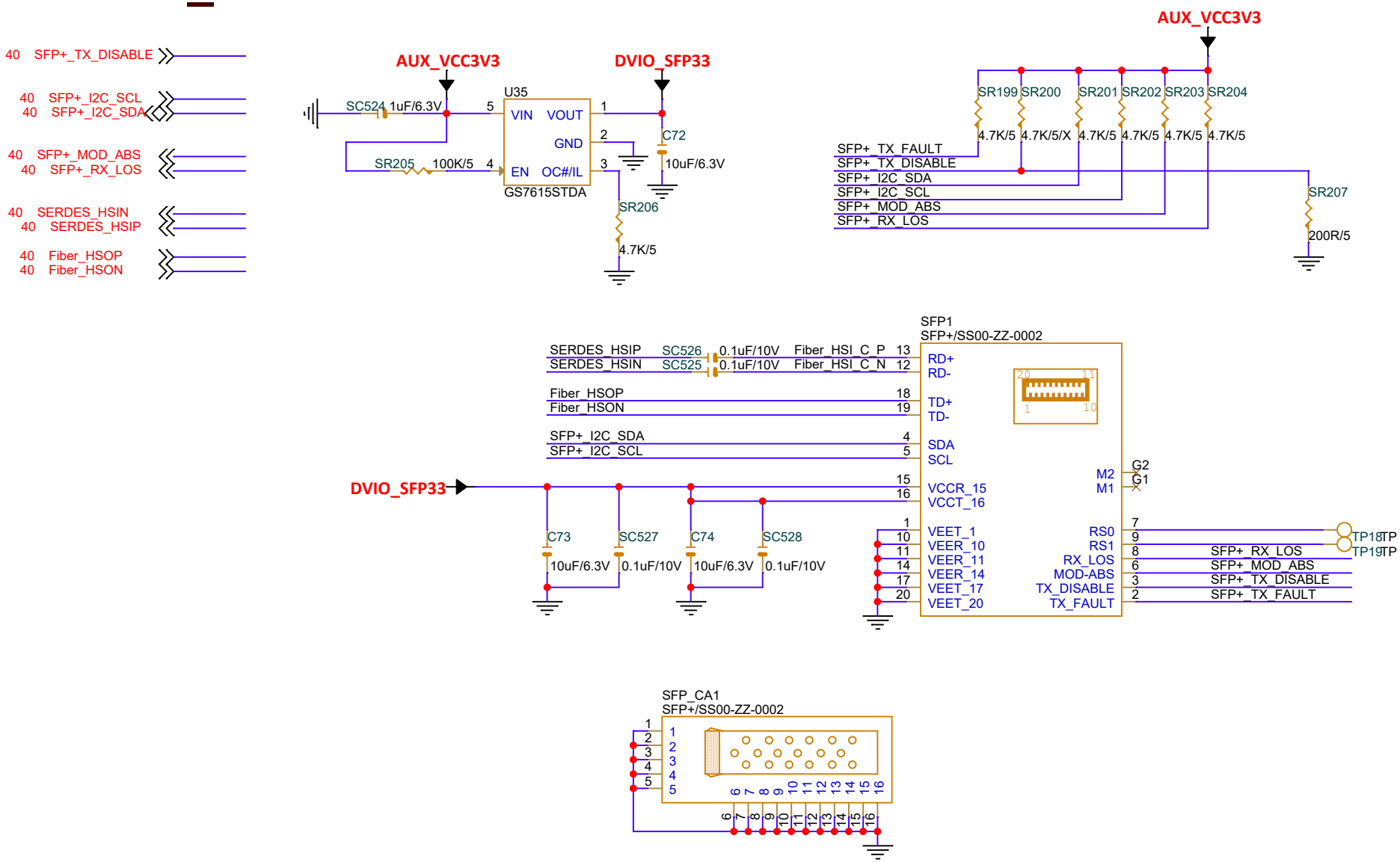
Ethernet_10G-SFP+



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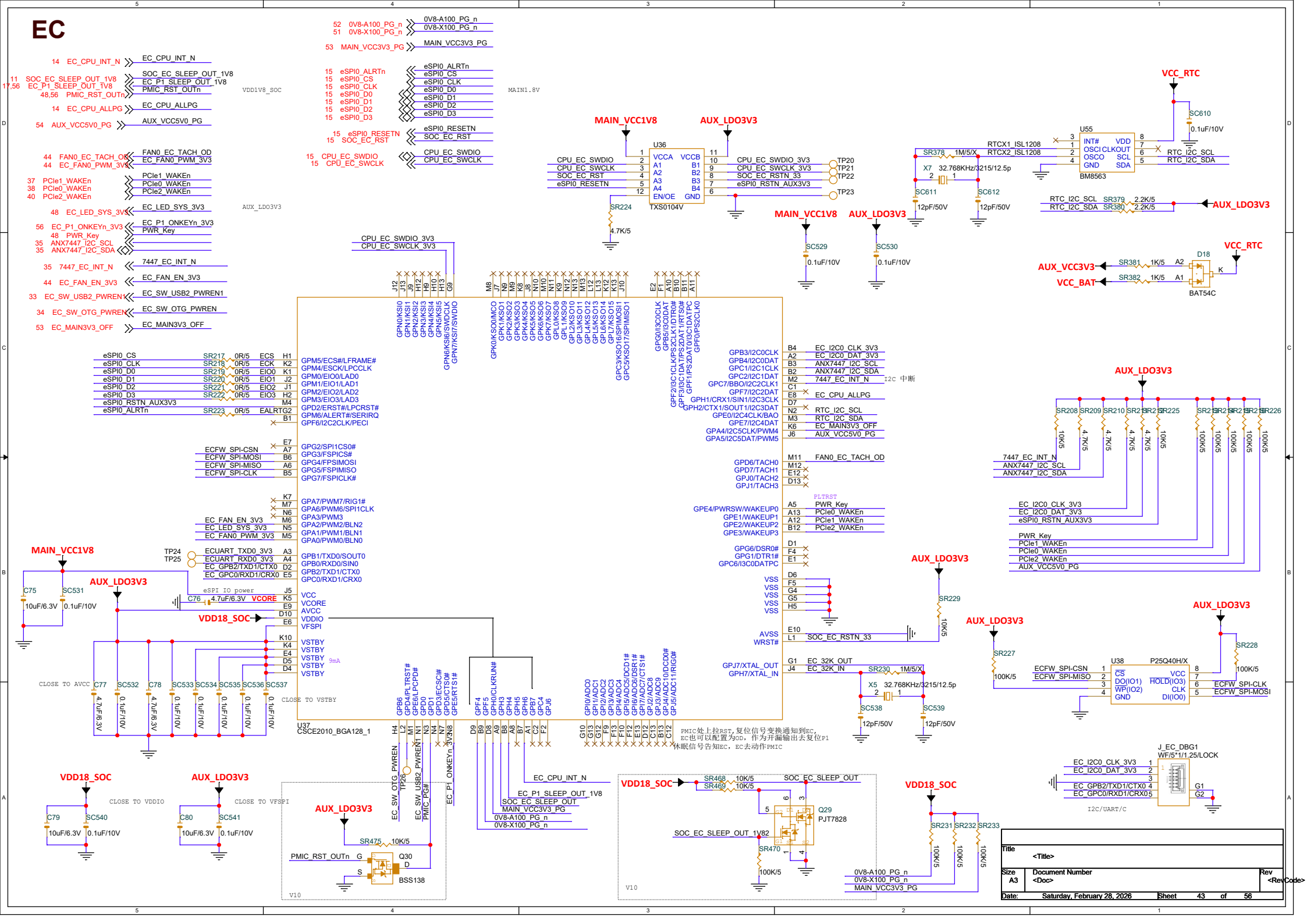
EC



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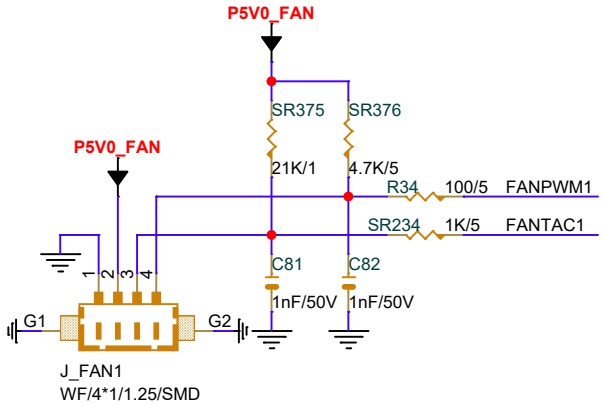
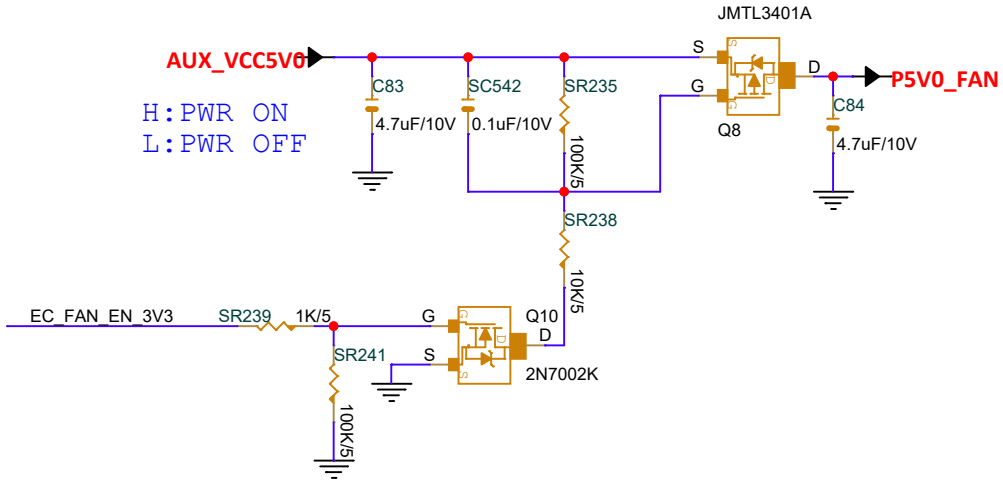
070 FAN

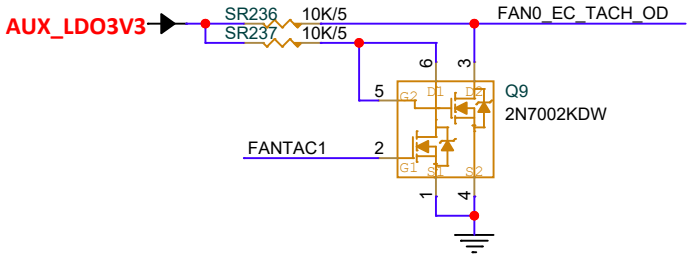
FAN

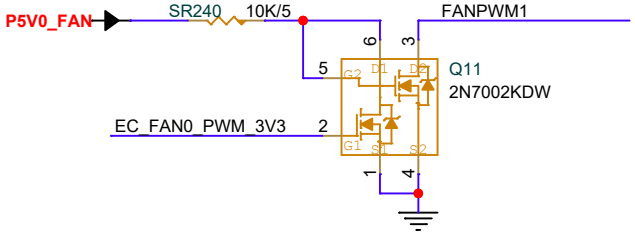
43 EC_FAN_EN_3V3
43 FAN0_EC_TACH_OD
43 EC_FAN0_PWM_3V3

EC_FAN_EN_3V3
FAN0_EC_TACH_OD
EC_FAN0_PWM_3V3









Title	<Title>	
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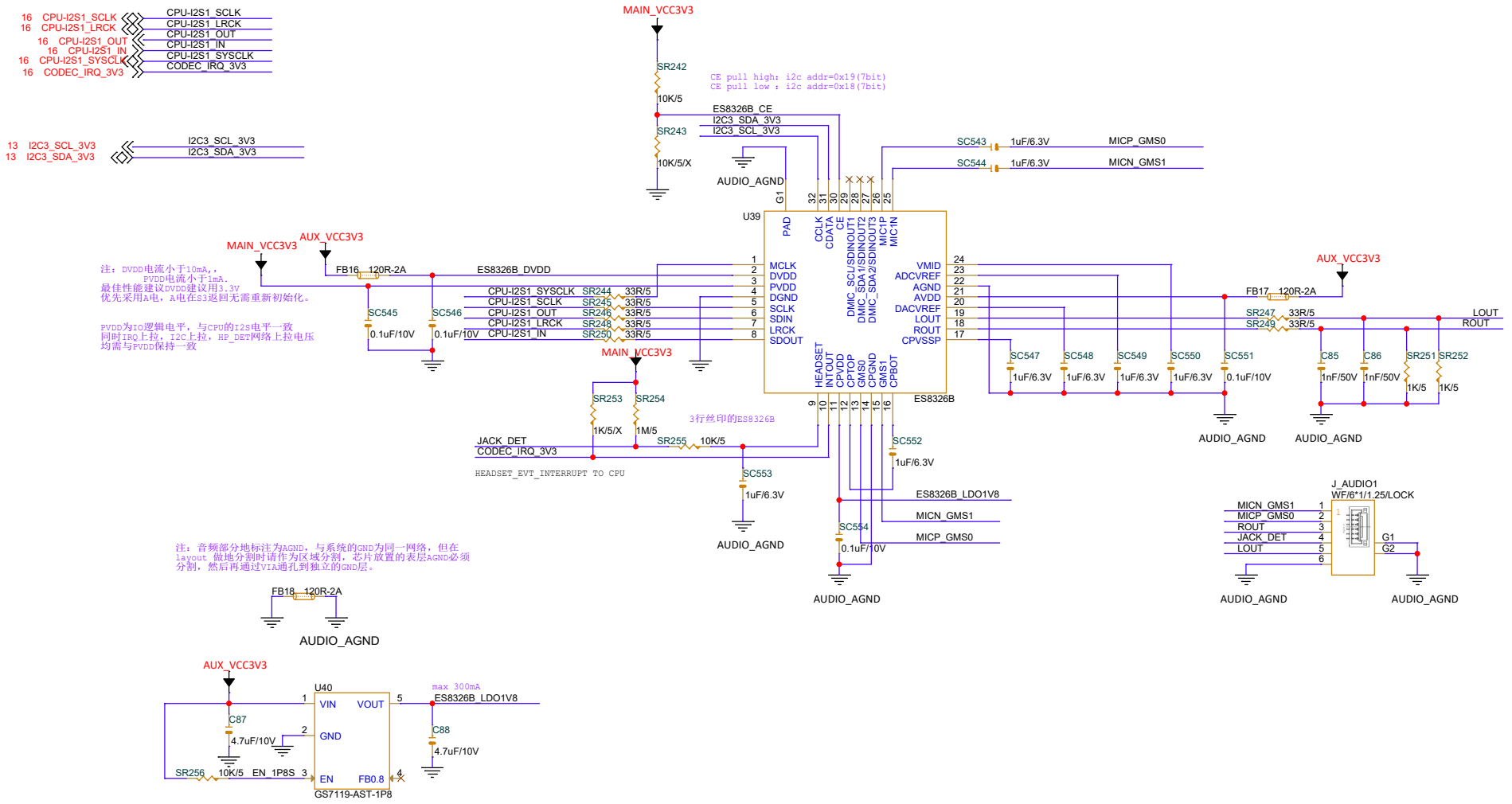
Audio Codec



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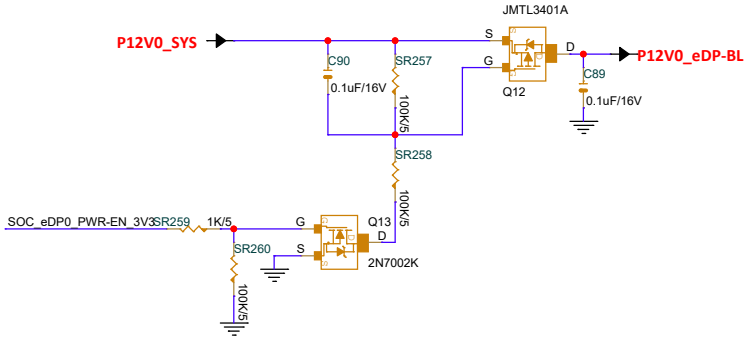
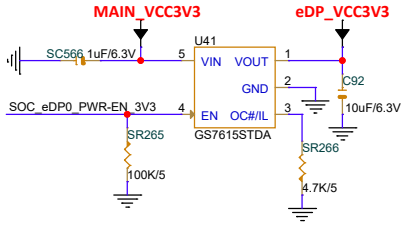
VO-eDP

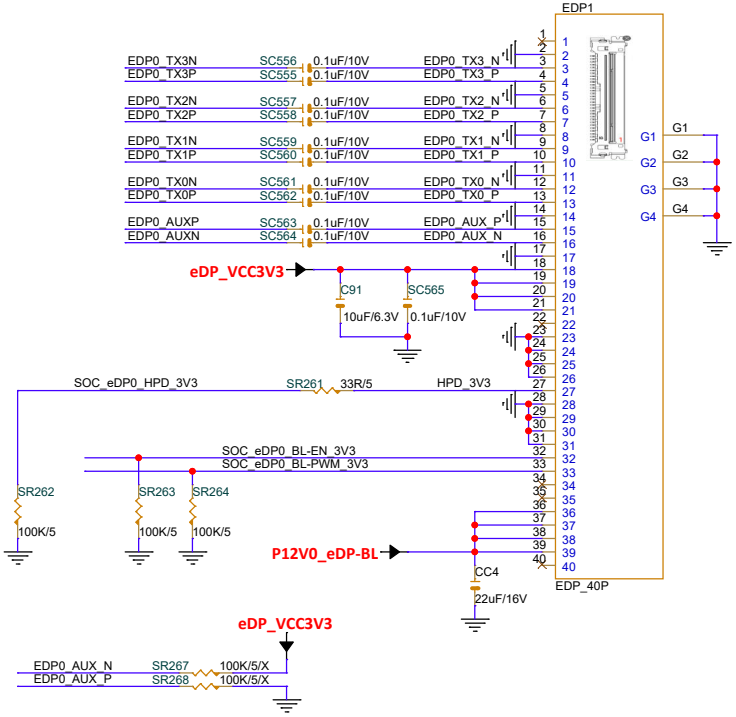
19 EDP0_AUXN
19 EDP0_AUXP

19 EDP0_TX0N
19 EDP0_TX0P
19 EDP0_TX1N
19 EDP0_TX1P
19 EDP0_TX2N
19 EDP0_TX2P
19 EDP0_TX3N
19 EDP0_TX3P

16 SOC_eDP0_BL-EN_3V3
16 SOC_eDP0_BL-PWM_3V3
13 SOC_eDP0_HPD_3V3
16 SOC_eDP0_PWR-EN_3V3







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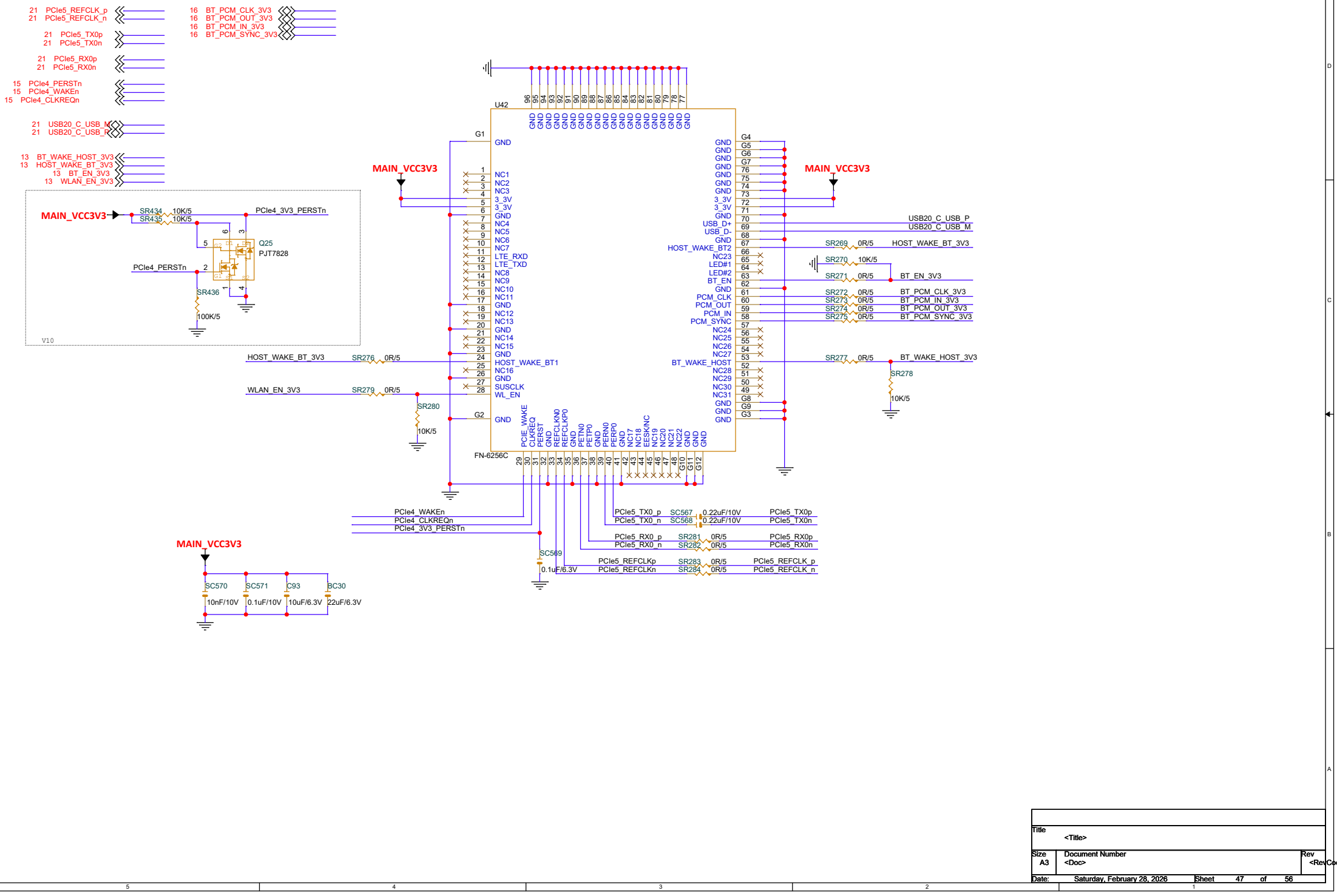
WIFI_FN-6256C



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Extend IO

R-GMAC3_TXD0 14
R-GMAC3_TXD1 14
R-GMAC3_TXD2 14
R-GMAC3_TXD3 14
R-GMAC3_TXEN 14
R-GMAC3_TXCLK 14

R-GMAC3_RXD0 14
R-GMAC3_RXD1 14
R-GMAC3_RXD2 14
R-GMAC3_RXD3 14
R-GMAC3_RXDV 14
R-GMAC3_RXCLK 14

R-GMAC3_REF0_CLK_25M 14

R-GMAC3_MDC 14
R-GMAC3_MDIO 14

R-GMAC3_RSTn_L 14
R-GMAC3_INT_N 14
GPIO

R-GMAC3_CRS 14
R-GMAC3_COL 14

R-CAN2_TXD_3V3 16
R-CAN2_RXD_3V3 16

R-CAN3_TXD_3V3 16
R-CAN3_RXD_3V3 16

R-CAN4_TXD_3V3 16
R-CAN4_RXD_3V3 16

UART5_TXD_3V3 13
UART5_RXD_3V3 13

UART10_TXD_3V3 13
UART10_RXD_3V3 13
UART10_CTS_3V3 13
UART10_RTS_3V3 13

13 R-I2C1_SCL_3V3
13 R-I2C1_SDA_3V3
R-I2C1_SCL_3V3
R-I2C1_SDA_3V3

14 SPI0_MOSI_1V8
14 SPI0_MISO_1V8
14 SPI0_SCLK_1V8
14 SPI0_CS_1V8
14 R-CAN0_RXD_1V8
14 R-CAN0_TXD_1V8
SPI0_MOSI_1V8
SPI0_MISO_1V8
SPI0_SCLK_1V8
SPI0_CS_1V8
R-CAN0_RXD_1V8
R-CAN0_TXD_1V8

16 R-UART0_TXD_3V3
16 R-UART0_RXD_3V3
R-UART0_TXD_3V3
R-UART0_RXD_3V3

13 R-PWM1_3V3
13 R-PWM2_3V3
R-PWM1_3V3
R-PWM2_3V3

14 CAN1_RXD_1V8
14 CAN1_TXD_1V8
CAN1_RXD_1V8
CAN1_TXD_1V8

R_CPU DEBUG

MAIN_VCC3V3
J1
R-I2C1_SCL_3V3
R-I2C1_SDA_3V3
R-UART0_TXD_3V3
R-UART0_RXD_3V3
UART5_TXD_3V3
UART5_RXD_3V3
R-PWM1_3V3
R-PWM2_3V3
R-CAN4_TXD_3V3
R-CAN4_RXD_3V3
R-CAN3_TXD_3V3
R-CAN3_RXD_3V3
R-CAN2_TXD_3V3
R-CAN2_RXD_3V3
FPC-26P-V

MAIN_VCC1V8
J2
CAN1_RXD_1V8
CAN1_TXD_1V8
R-GMAC3_TXCLK
R-GMAC3_TXD0
R-GMAC3_TXD1
R-GMAC3_TXD2
R-GMAC3_TXD3
R-GMAC3_RXCLK
R-GMAC3_RXD0
R-GMAC3_RXD1
R-GMAC3_RXD2
R-GMAC3_RXD3
R-GMAC3_TXEN
R-GMAC3_REF0_CLK_25M
R-GMAC3_RXDV
R-GMAC3_INT_N
R-GMAC3_RSTn_L
R-GMAC3_MDC
R-GMAC3_MDIO
R-GMAC3_CRS
R-GMAC3_COL
SPI0_MOSI_1V8
SPI0_MISO_1V8
SPI0_SCLK_1V8
SPI0_CS_1V8
R-CAN0_RXD_1V8
R-CAN0_TXD_1V8
FPC-36P-V

X100 DEBUG

1V8_ALDO_ON
AUX_VCC3V3
V10
SR285 10K/5
SR286 10K/5
SR287 10K/5/X
SR288 10K/5/X
11 UART0_TXD_PMU
11 UART0_RXD_PMU
UART0_TXD_PMU
UART0_RXD_PMU
Q14
PJT7828
SR476 33R/5
SR477 33R/5
C208 330pF/50V
C209 330pF/50V
J_UART_DBG1
HDR/3*1/2.54
UART0_TXD_3V3
UART0_RXD_3V3

SYS_LED

43 EC_LED_SYS_3V3
J_LED1
WF/4*1/1.25/LOCK
SYS_LED_P
SYS_LED_N
PWR_BUTTON_P
AUX_VCC3V3
R64 510R/5
R35 1K/5
LED4
LED/G/0603
EC_LED_SYS_3V3
SR289 4.7K/5
Q15
2N7002K

POWER ON

SW2
SW/YST-1109L
PWR_BUTTON_P
SR290 33R/5 PWR_Key
PWR_Key 43
SR291 33R/5/XONKEYn_5V0
ONKEYn_5V0 56
D15
JEB05DF
SC572
0.1uF/10V

REST

SW3
SW/YST-1109L
PMIC处上拉RST
43,56 PMIC_RST_OUTn
PMIC_RST_OUTn SR292 33R/5
RESET_IN_N 11
D16
JEB05DF
SC573
0.1uF/10V

Title	<Title>	
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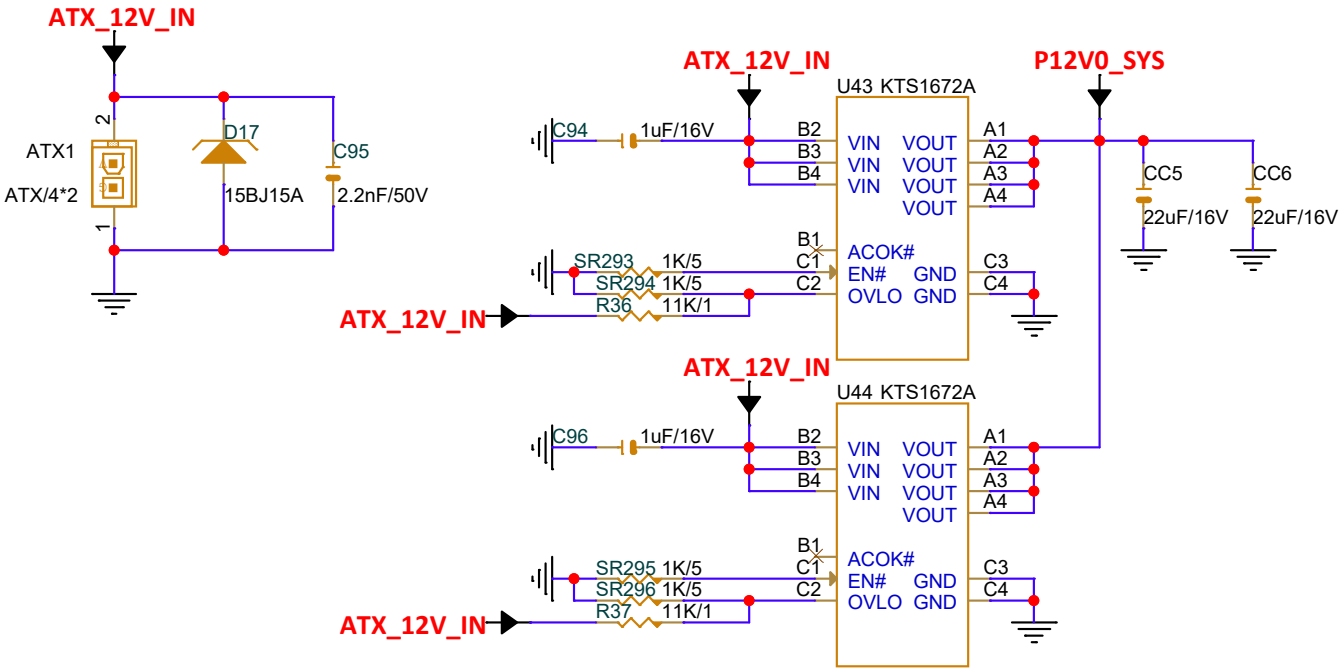
ATX_POWER



Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
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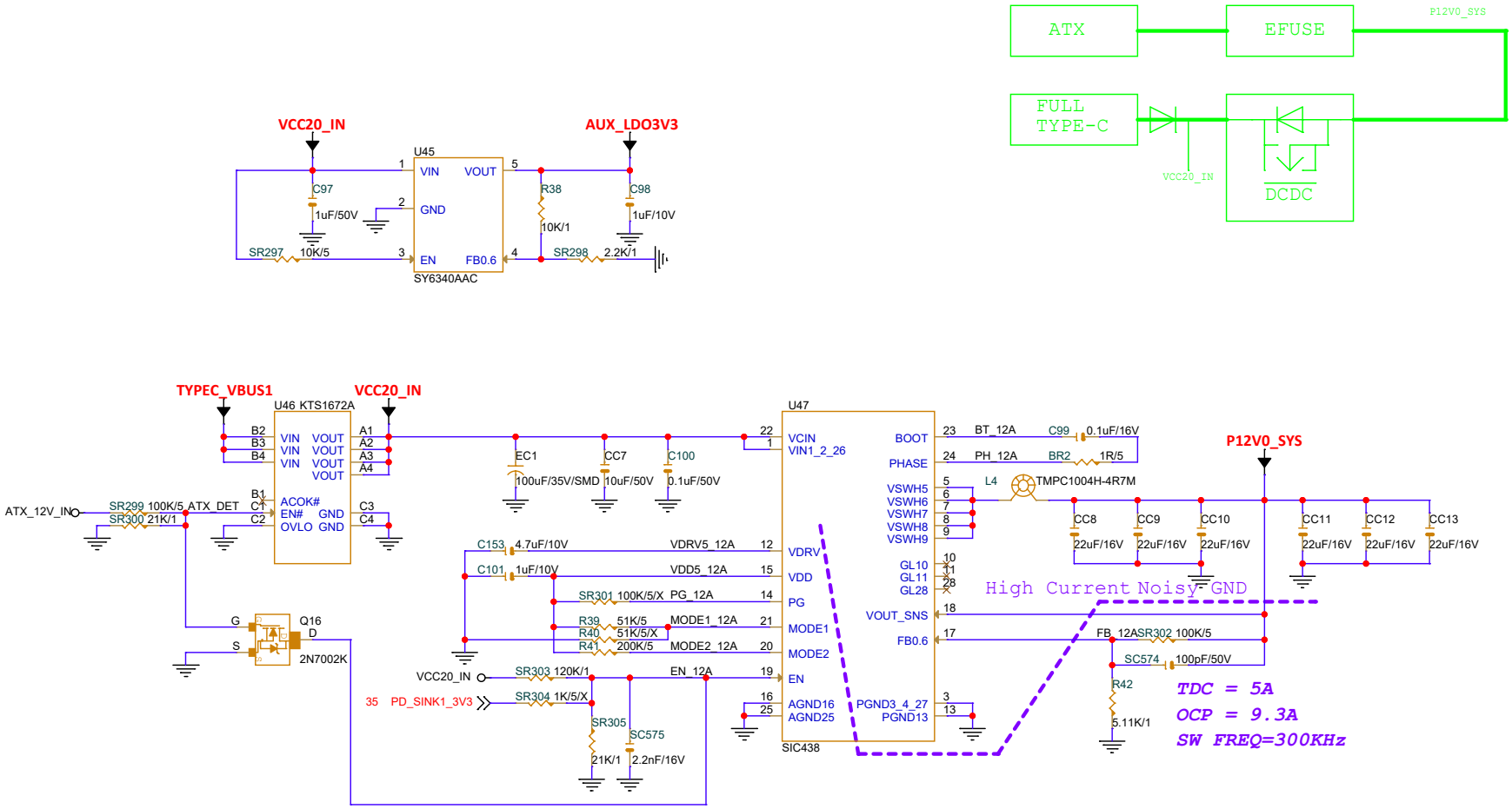

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
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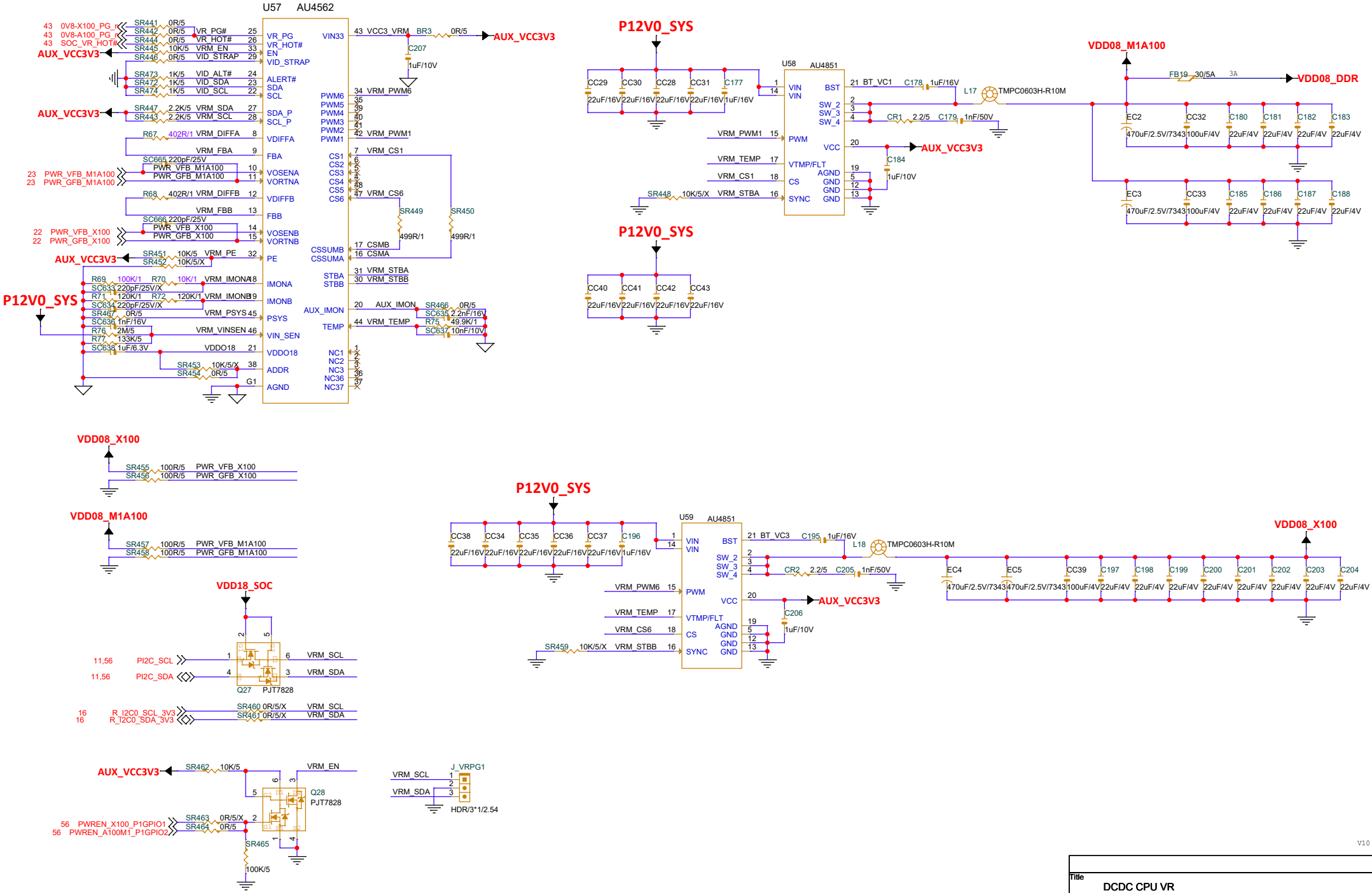
DCDC CPU VR



V10

Title	DCDC CPU VR		
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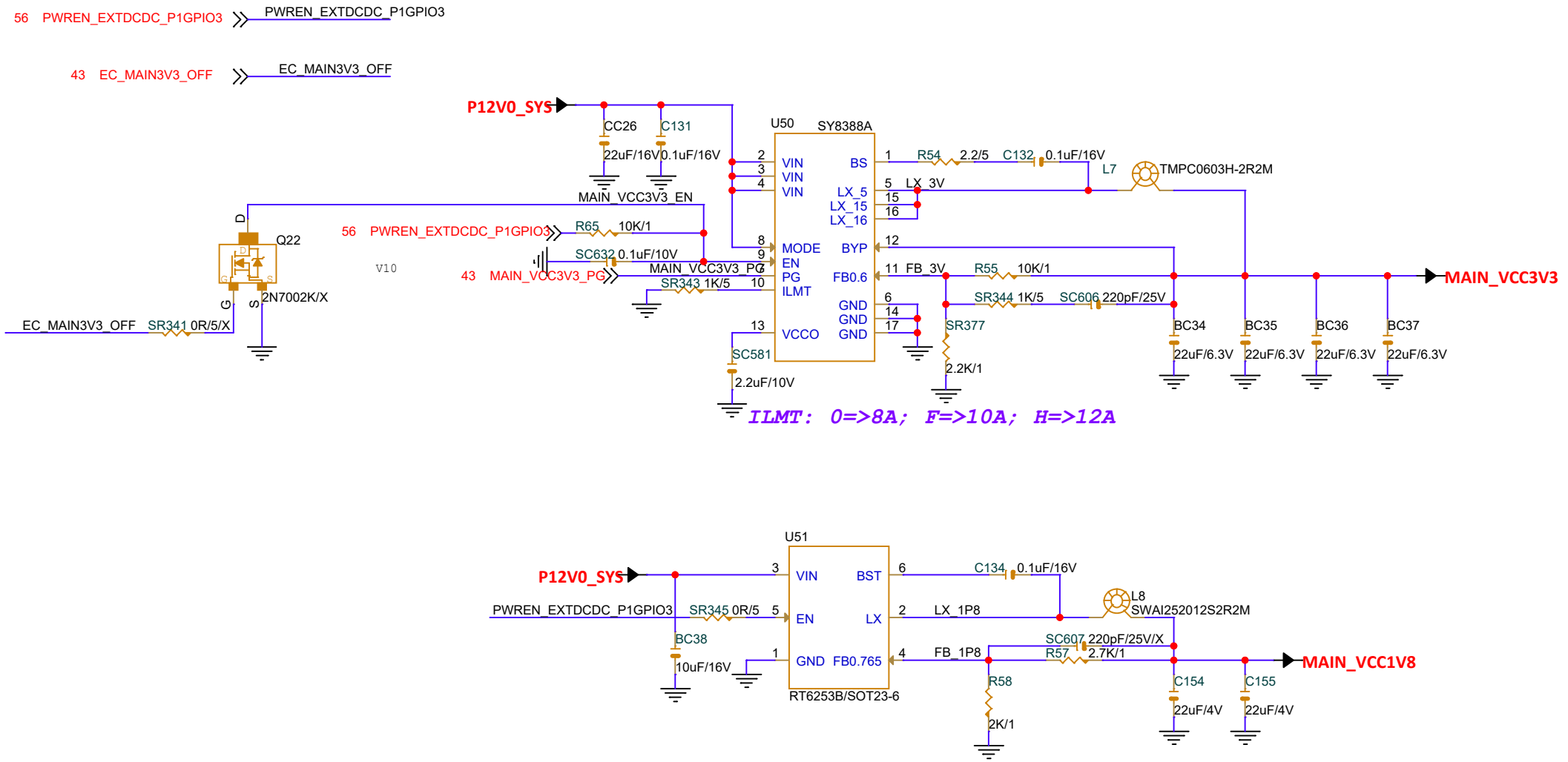
Power DCDC-MAIN



Title	<Title>	
Size A4	Document Number <Doc>	Rev <RevCo
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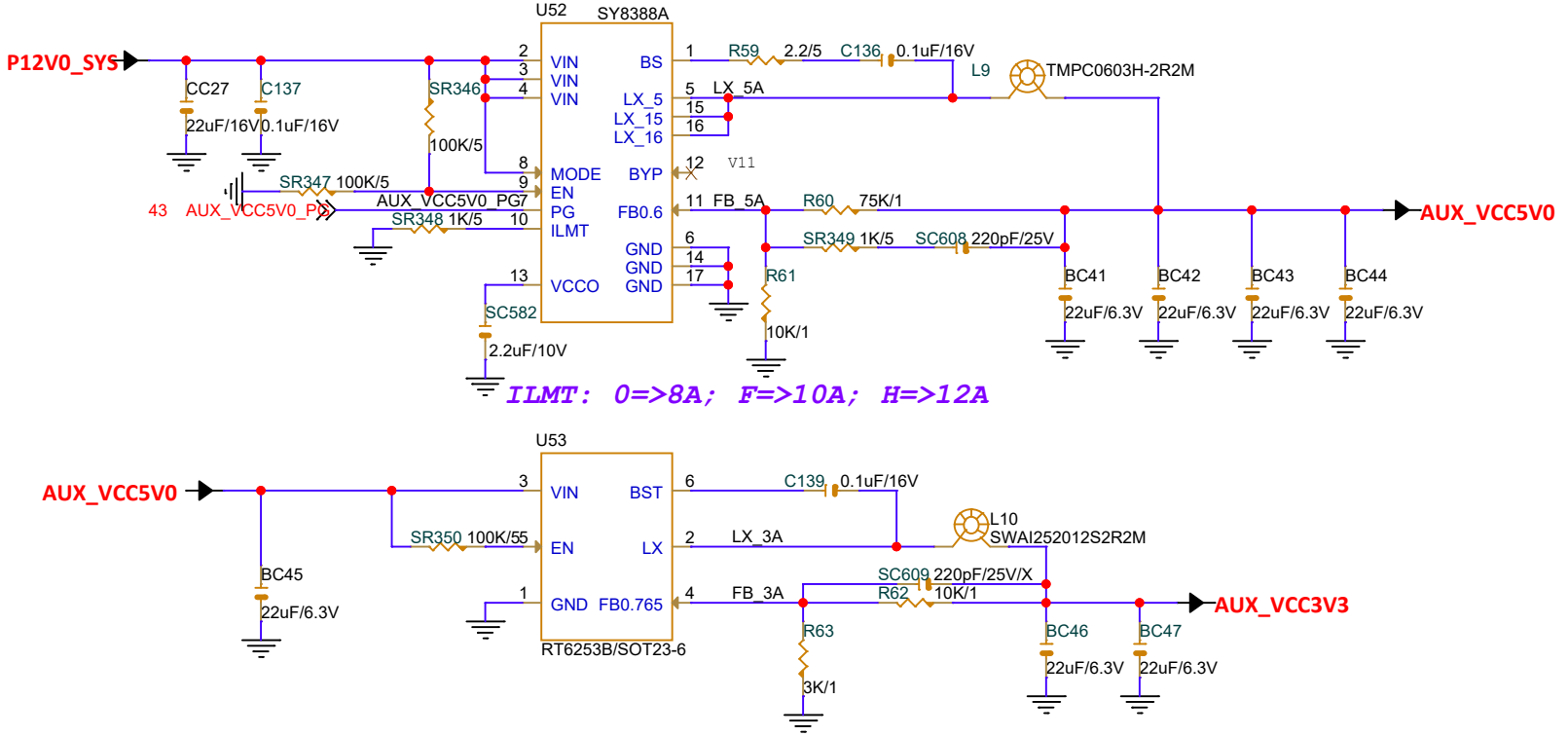
POWER_DCDC-AUX



Title	<Title>		
Size A4	Document Number <Doc>		Rev <RevCo
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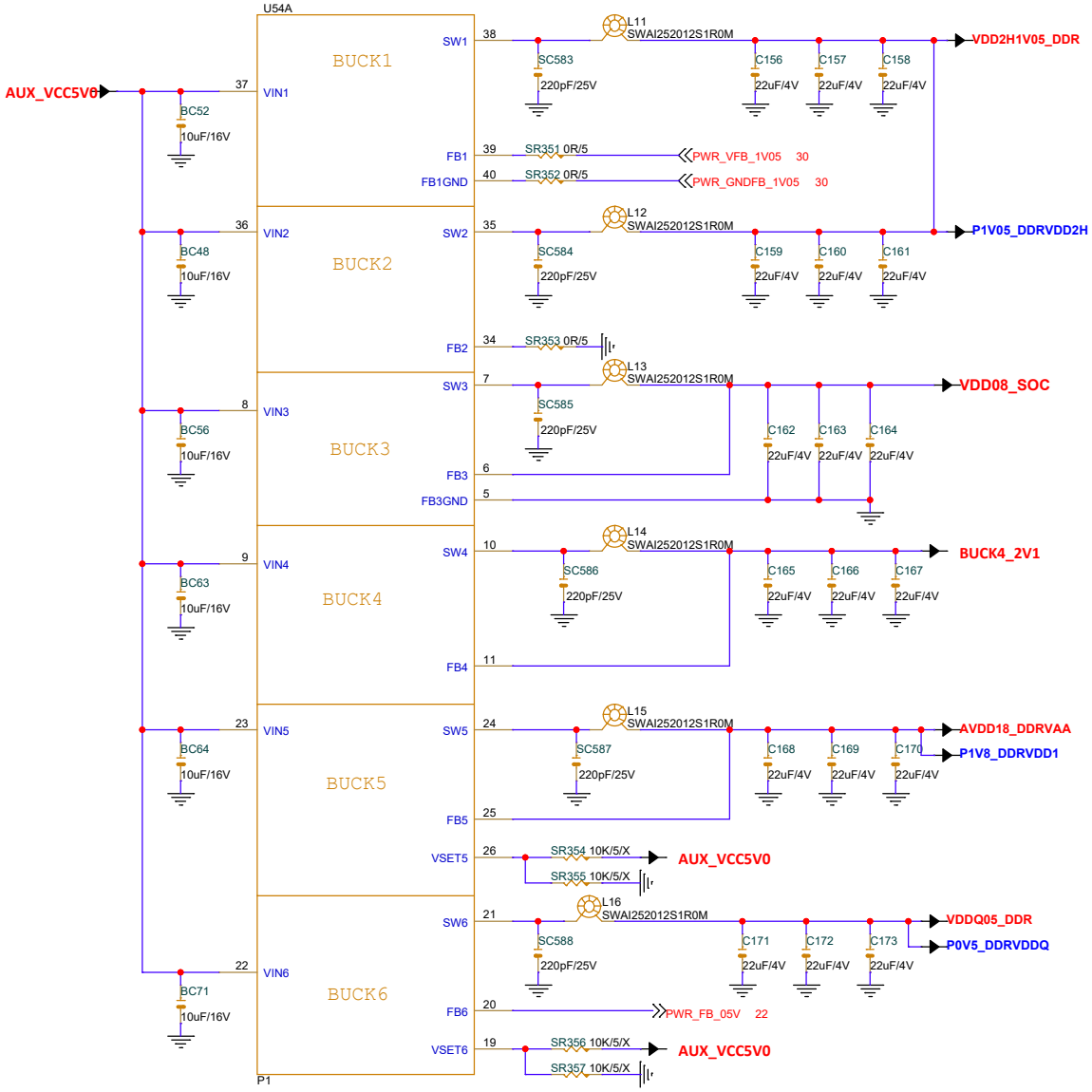
PMIC BUCK



Title	<Title>	
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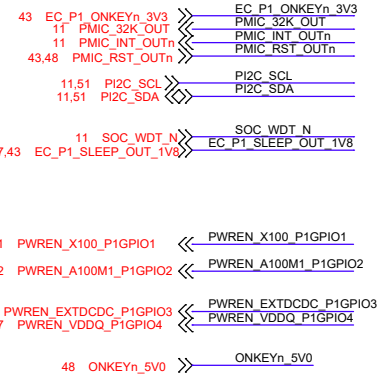
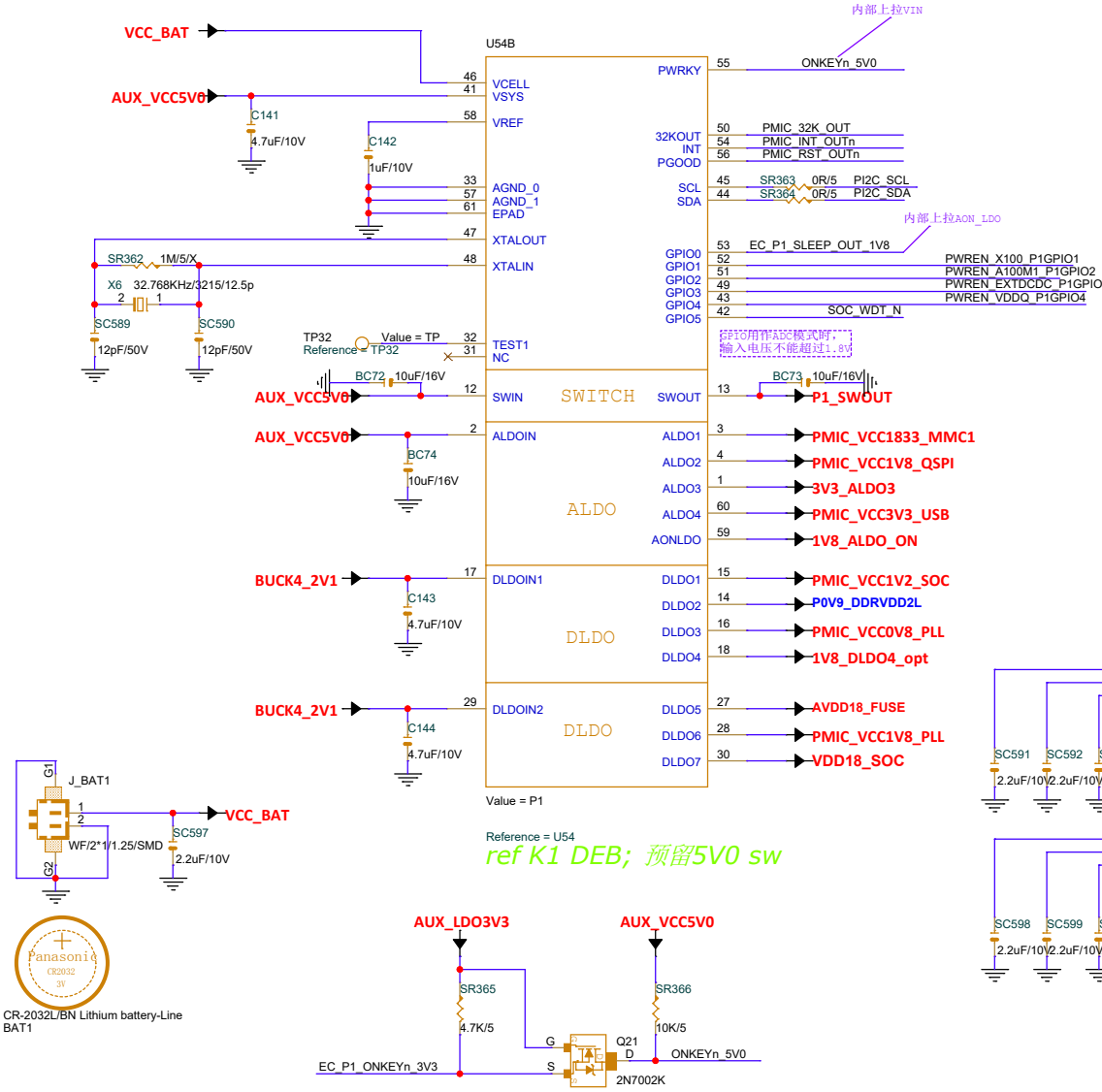
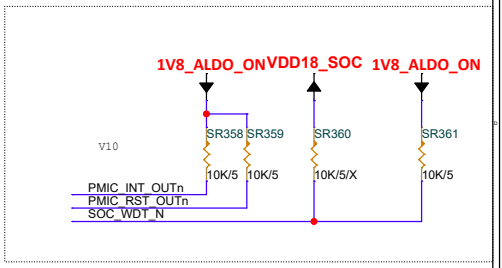
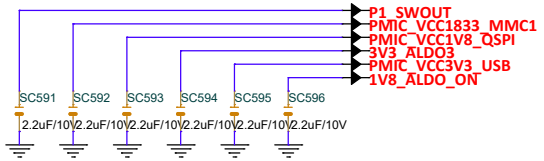
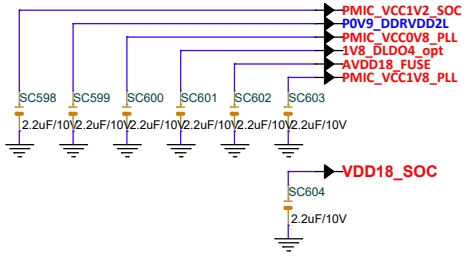
PMIC LDO & Contr











Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode
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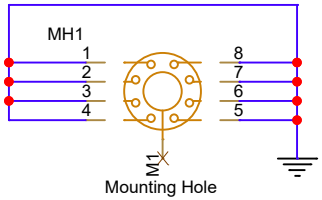

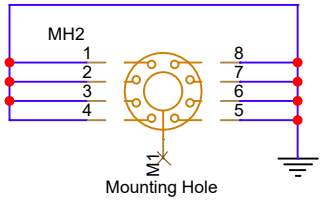

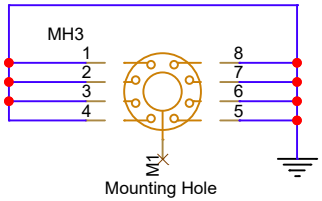

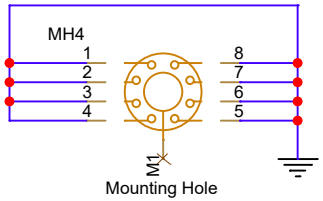

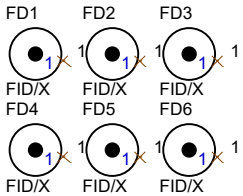

Title <Title>		
Size A4	Document Number <Doc>	Rev <RevC
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