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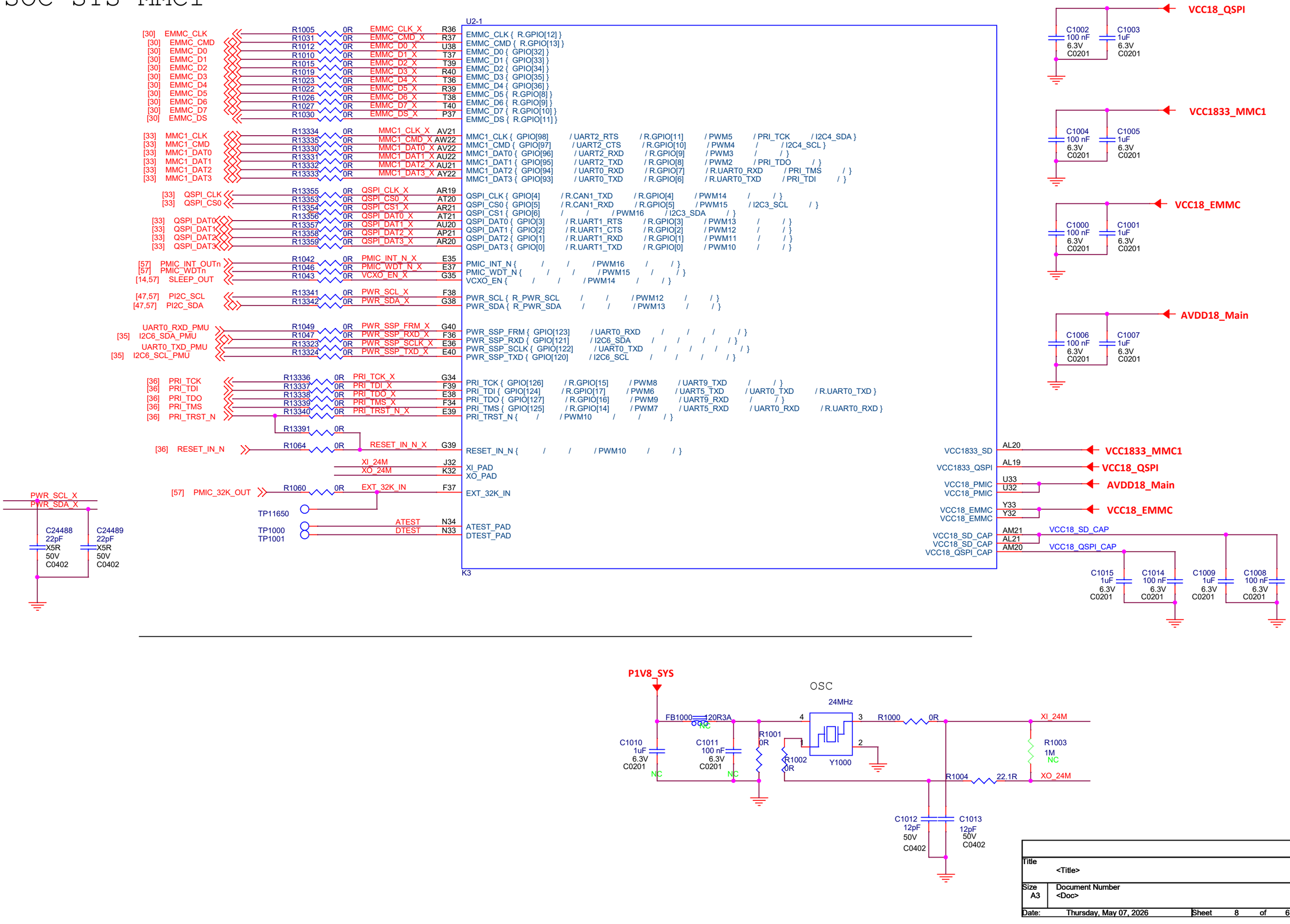

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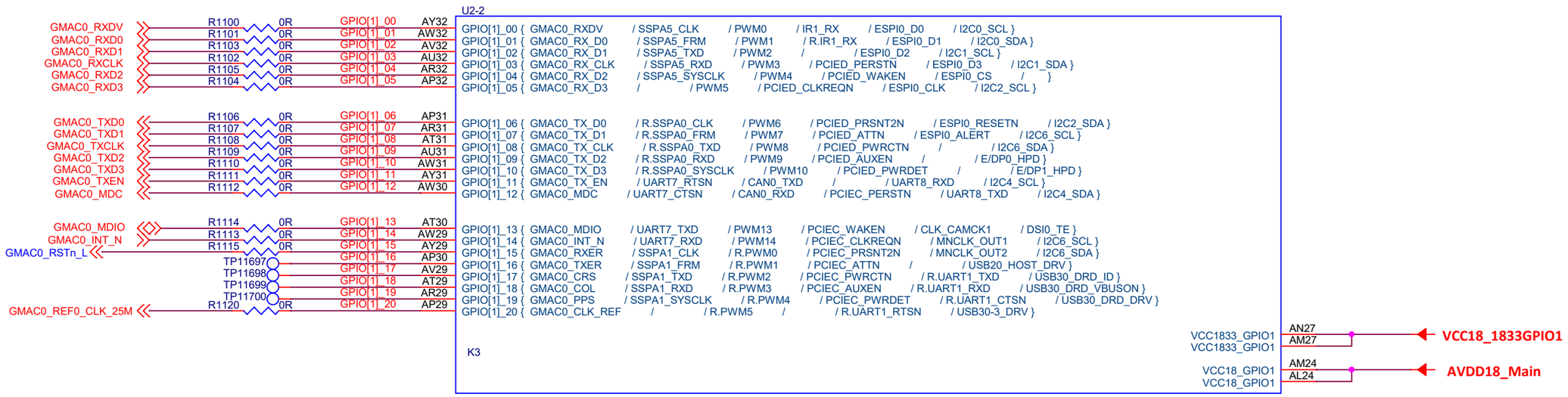

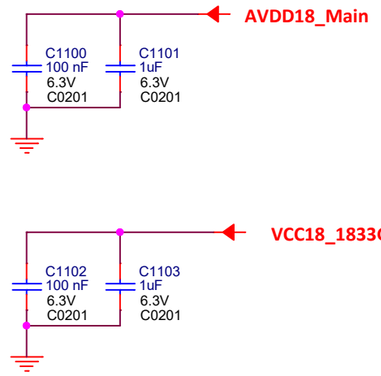

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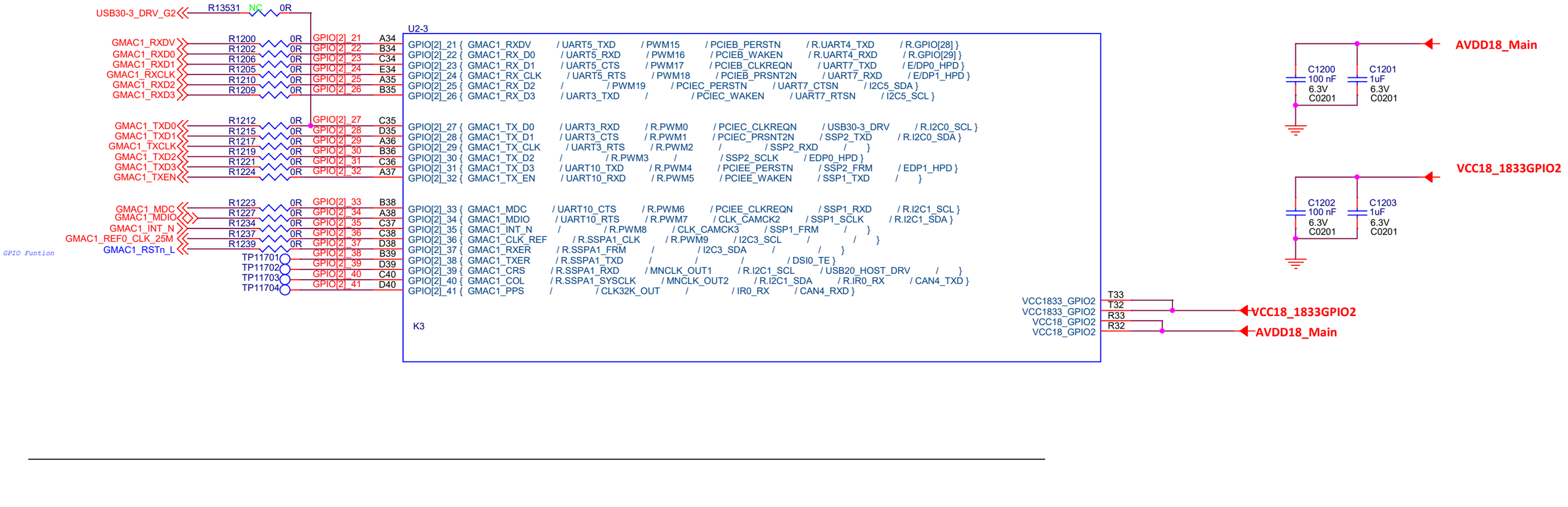

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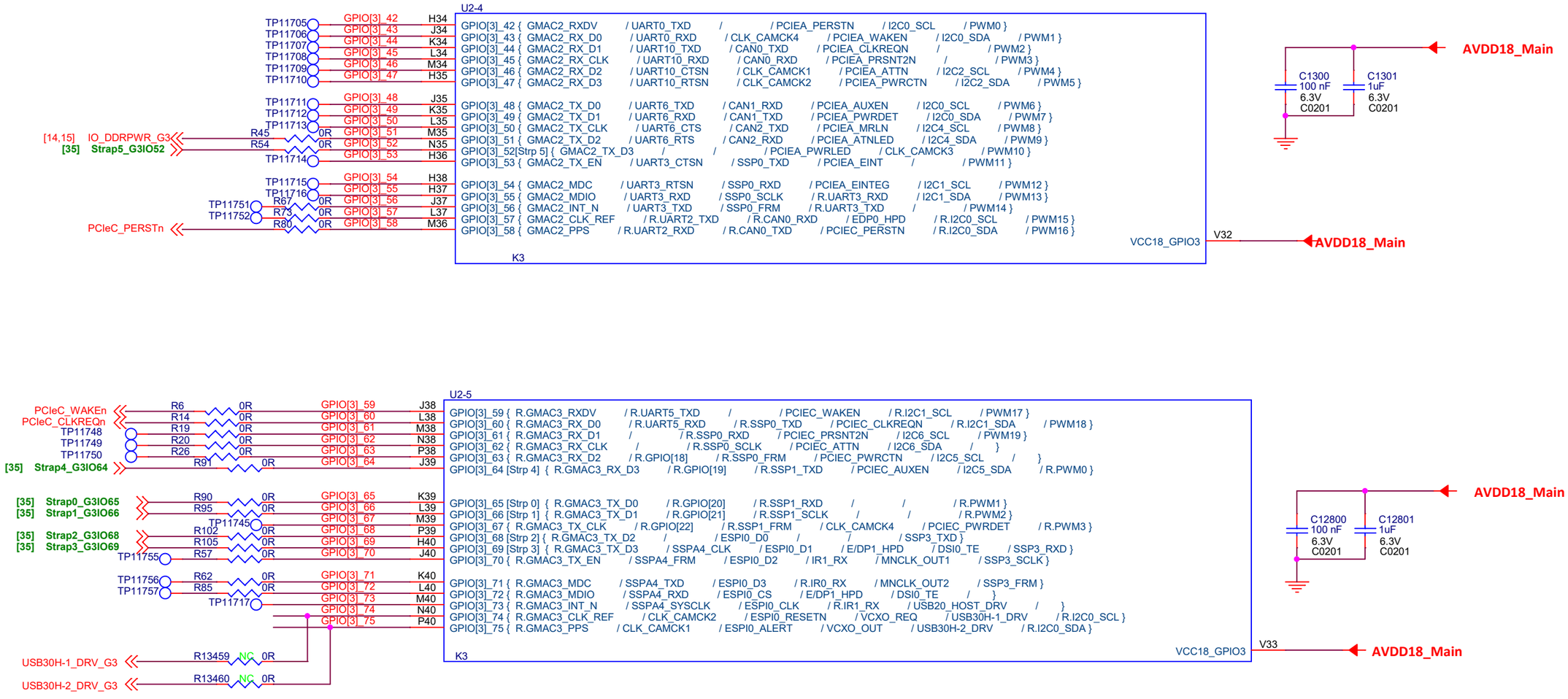

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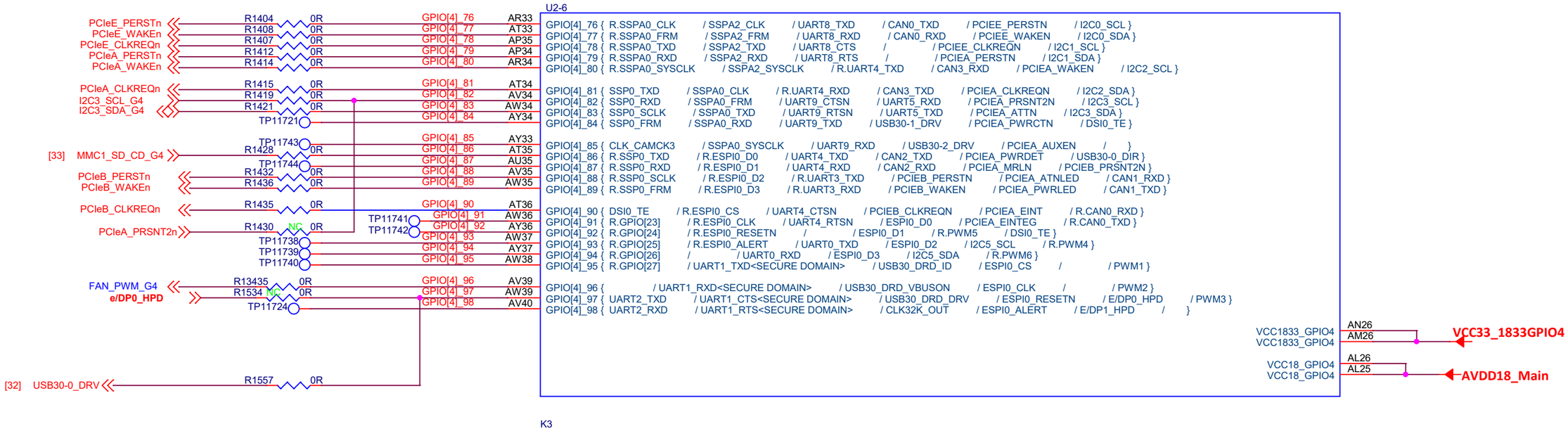
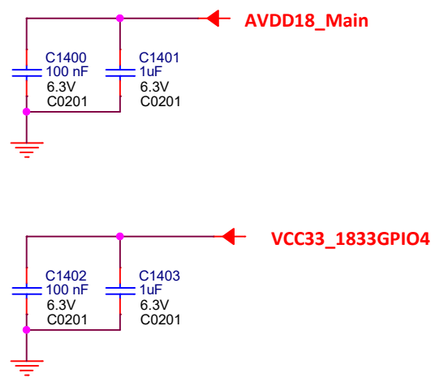
SOC-GPIO-4

3V3 Config

default 3.3 config



MuX function Test



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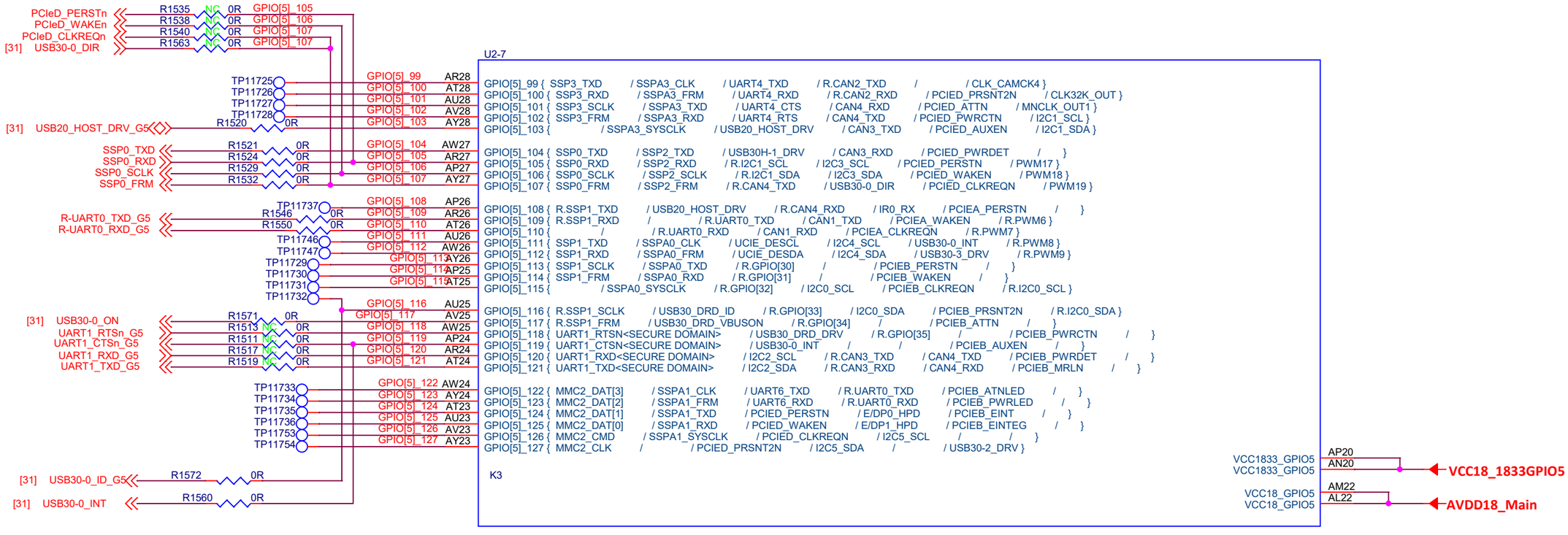
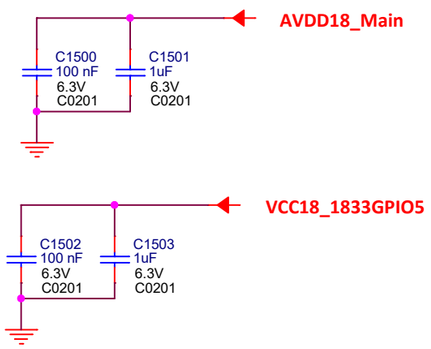
SOC-GPIO-5





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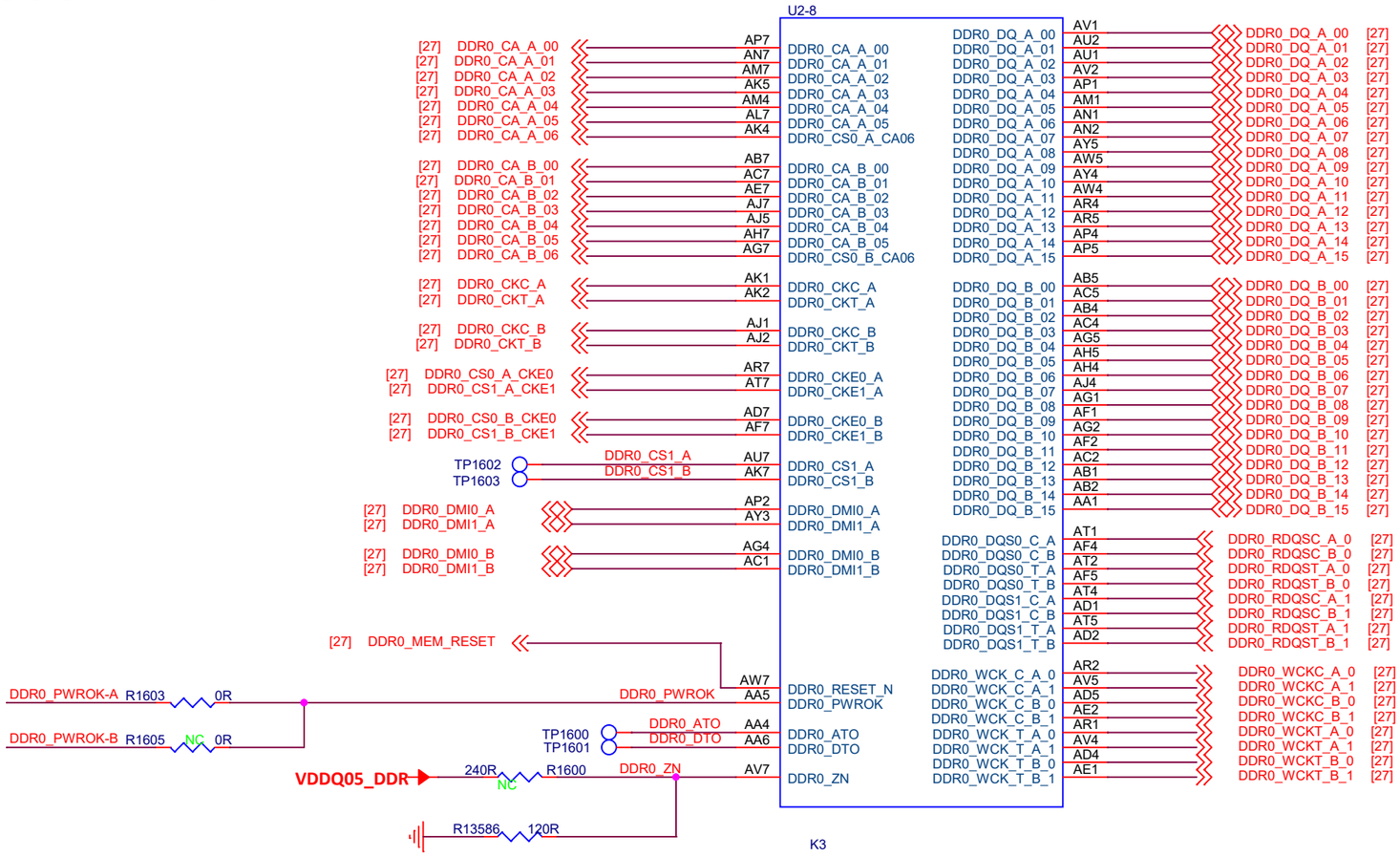
SOC-DDR0



DDR0&DDR1 LP5/LP4 Pin 复用如下

DDR1_CKE0_A	LP5_DDR1_CS0_A	LP4_DDR1_CKE0_A
DDR1_CKE0_B	LP5_DDR1_CS0_B	LP4_DDR1_CKE0_B
DDR1_CKE1_A	LP5_DDR1_CS1_A	LP4_DDR1_CKE1_A
DDR1_CKE1_B	LP5_DDR1_CS1_B	LP4_DDR1_CKE1_B

DDR1_CS0_A	LP5_DDR1_CA_A_06	LP4_DDR1_CS0_A
DDR1_CS0_B	LP5_DDR1_CA_B_06	LP4_DDR1_CS0_B
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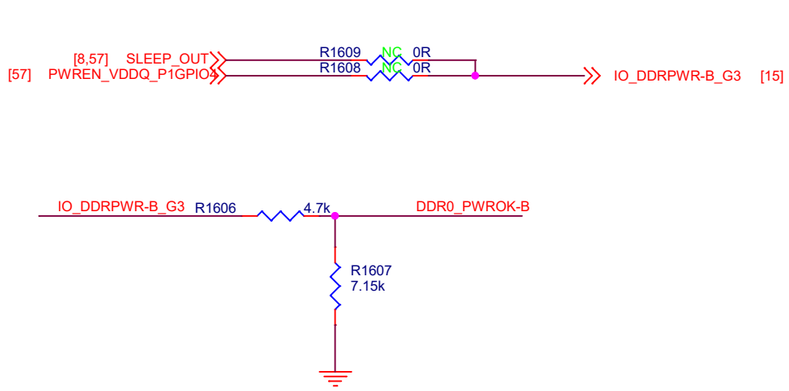
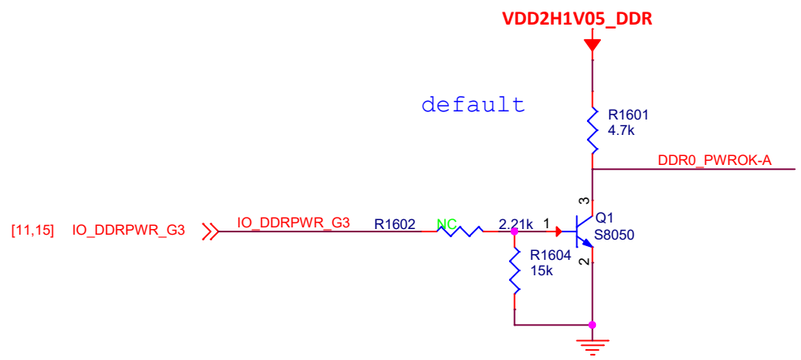
DDR1_CS1_B	NA	LP4_DDR1_CS1_B





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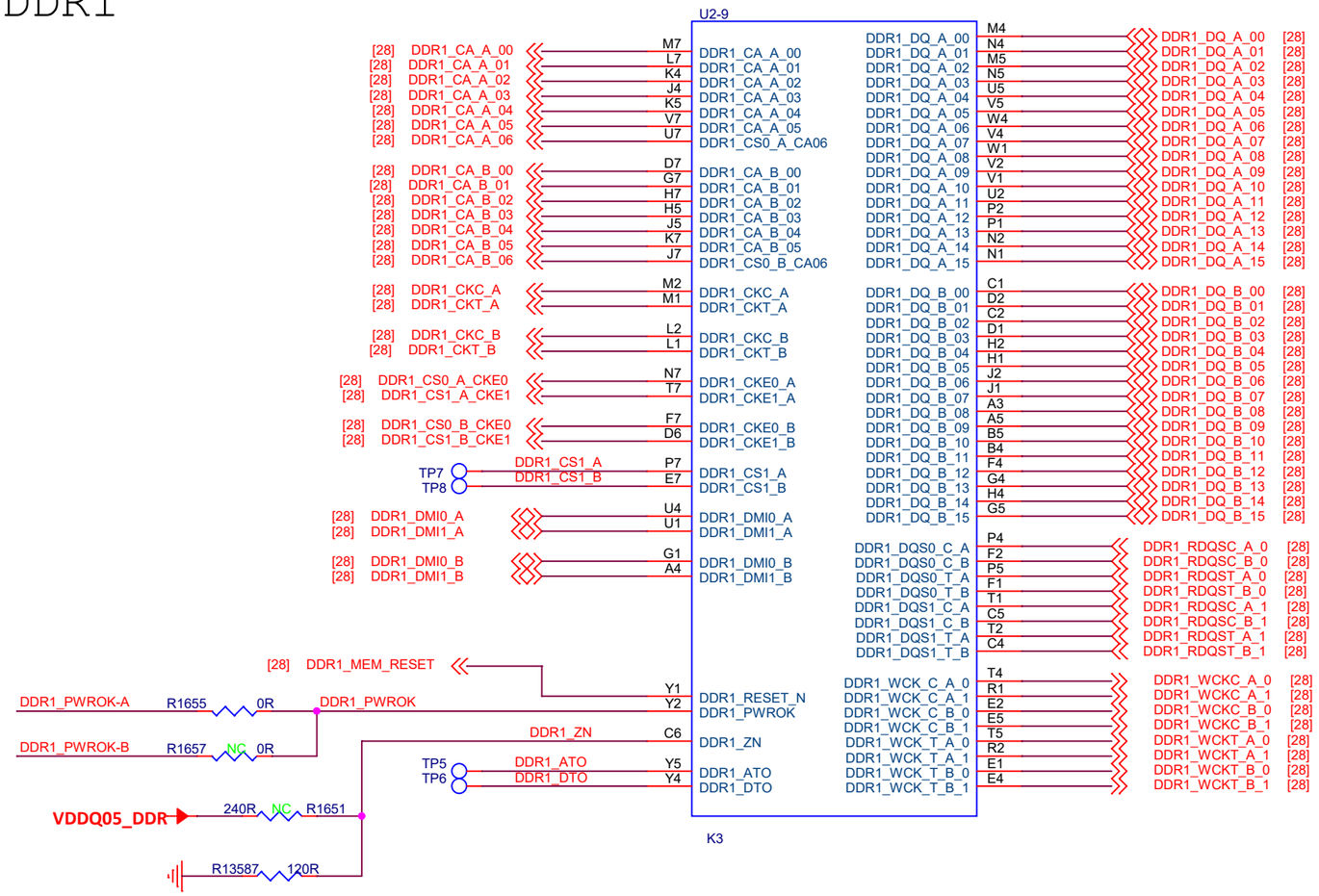
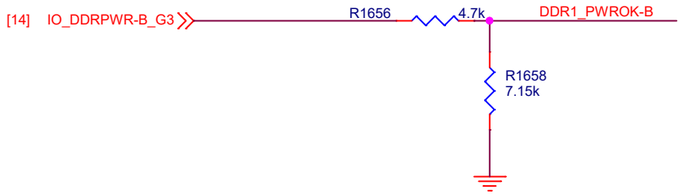
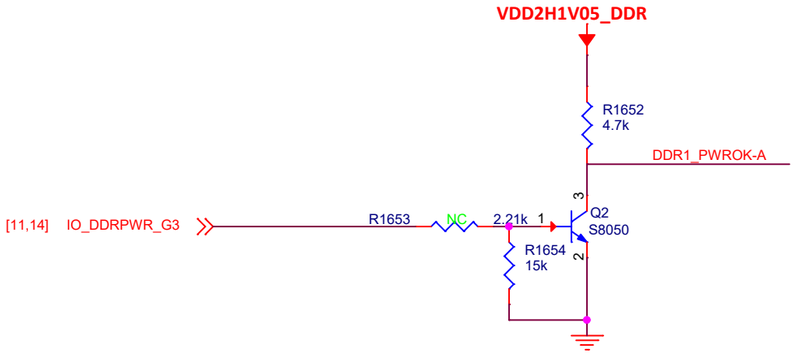
SOC-DDR1







DDR0&DDR1 LP5/LP4 Pin 复用如下

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DDR1_CKE0_B	LP5_DDR1_CS0_B	LP4_DDR1_CKE0_B
DDR1_CKE1_A	LP5_DDR1_CS1_A	LP4_DDR1_CKE1_A
DDR1_CKE1_B	LP5_DDR1_CS1_B	LP4_DDR1_CKE1_B

DDR1_CS0_A	LP5_DDR1_CA_A_06	LP4_DDR1_CS0_A
DDR1_CS0_B	LP5_DDR1_CA_B_06	LP4_DDR1_CS0_B
DDR1_CS1_A	NA	LP4_DDR1_CS1_A
DDR1_CS1_B	NA	LP4_DDR1_CS1_B

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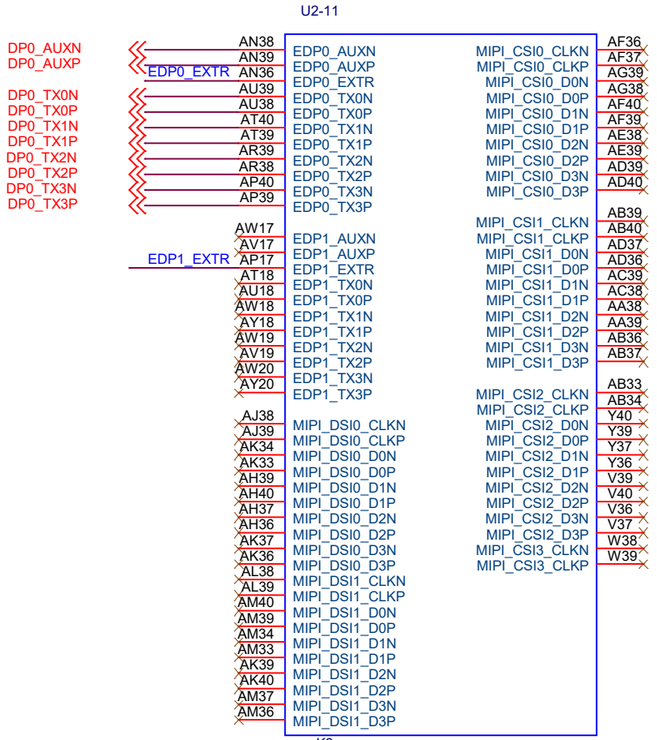
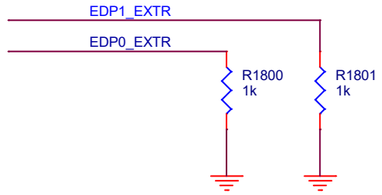
SOC-DSI-DP-CSI





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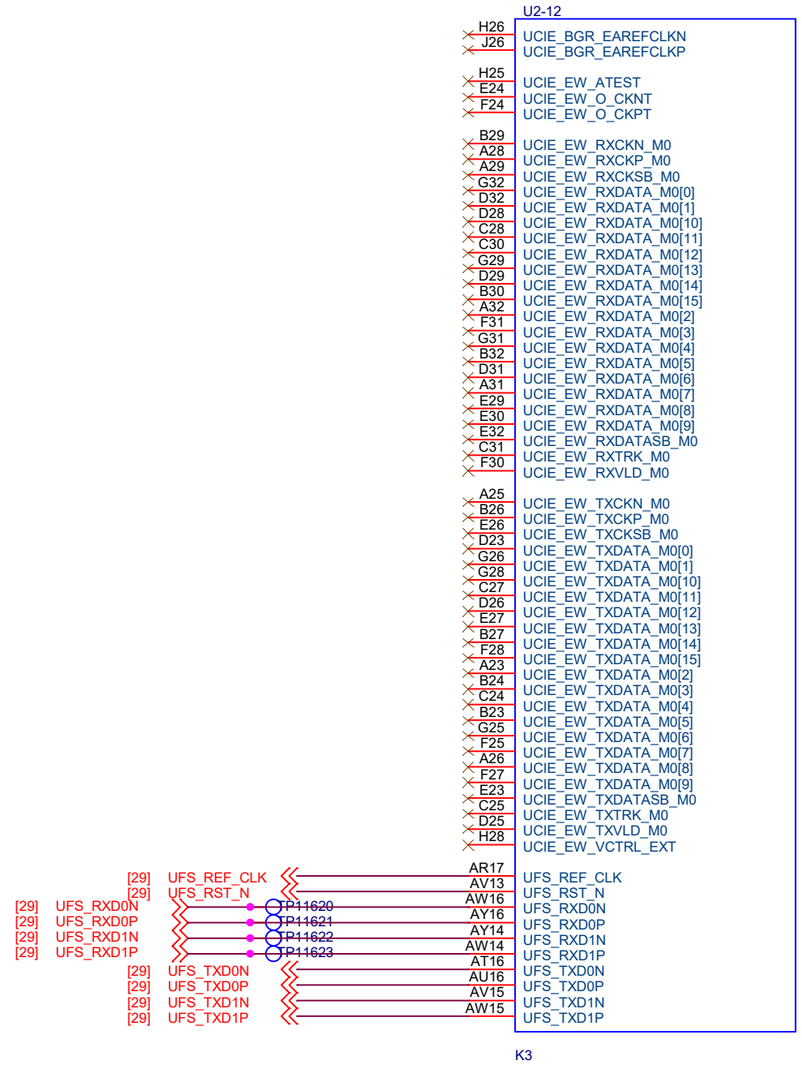

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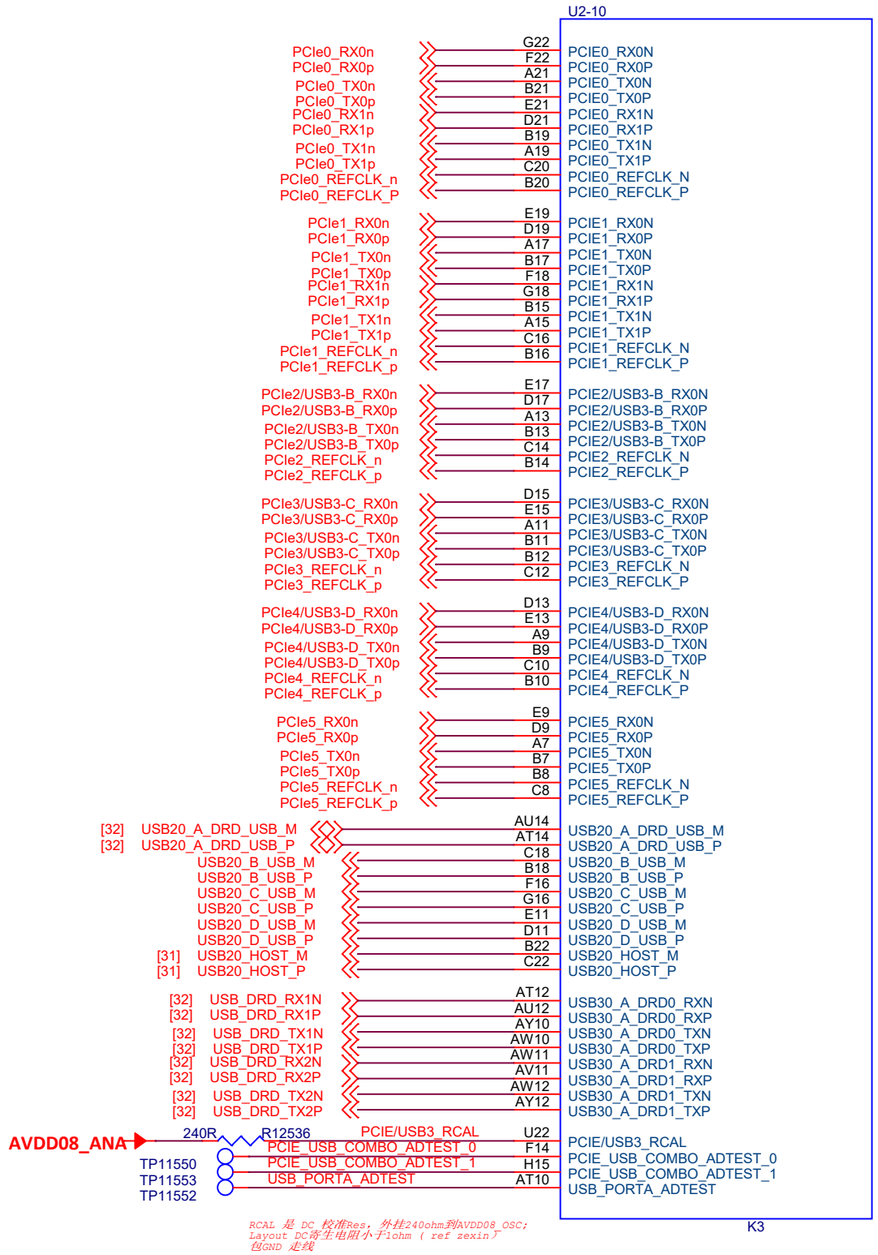

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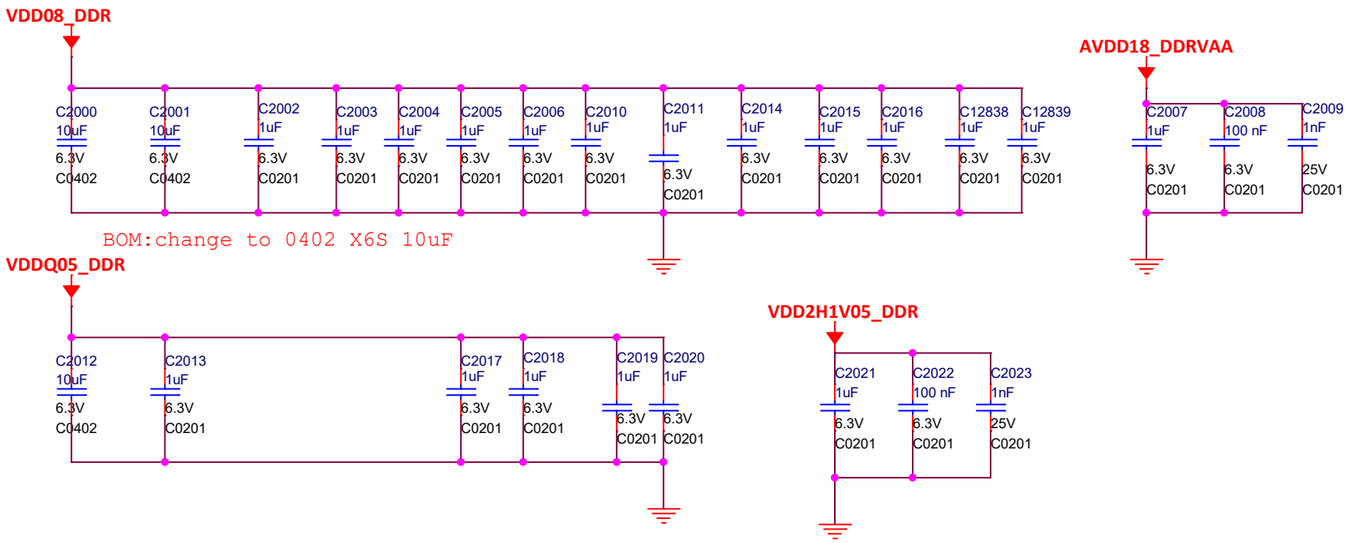
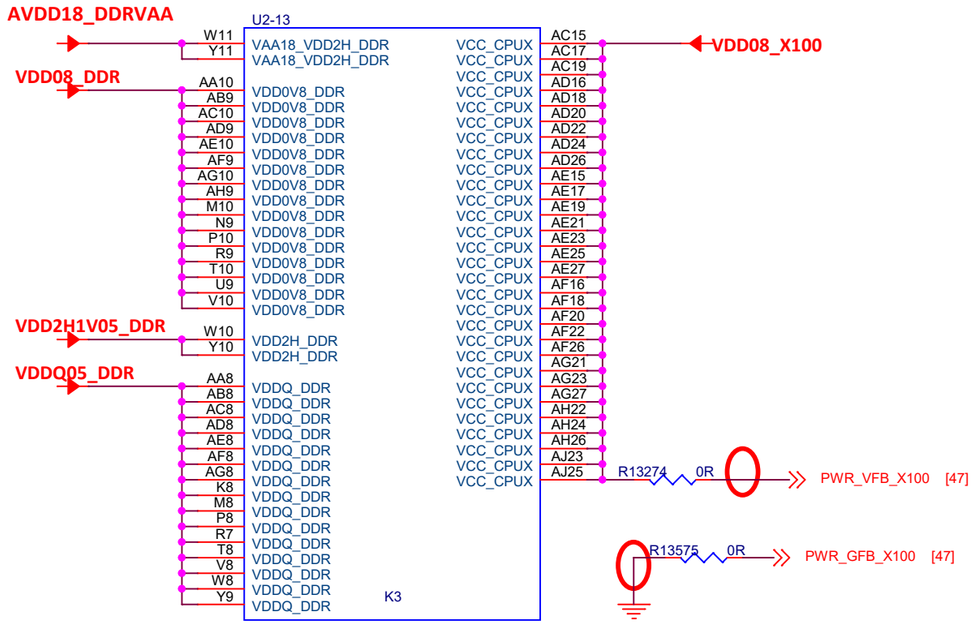
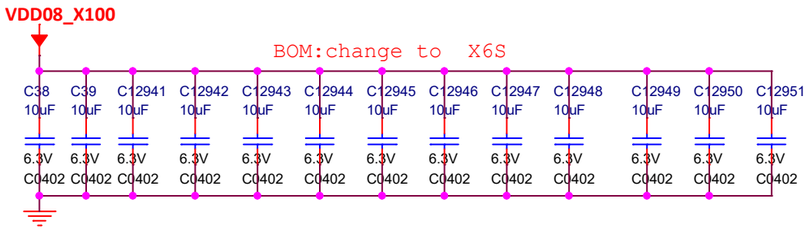
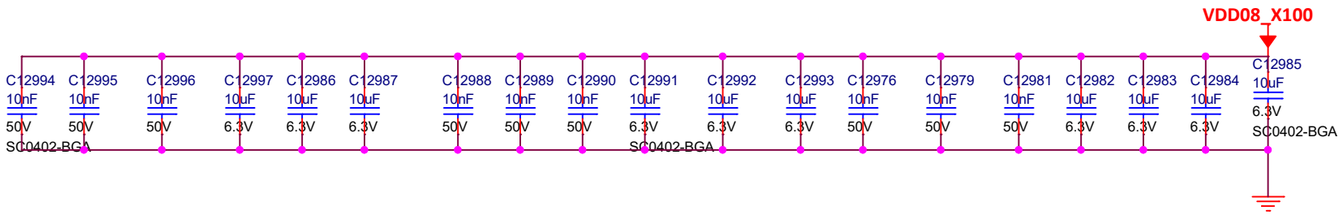
SOC-DDR PWR CAP





CPU X100 CAP





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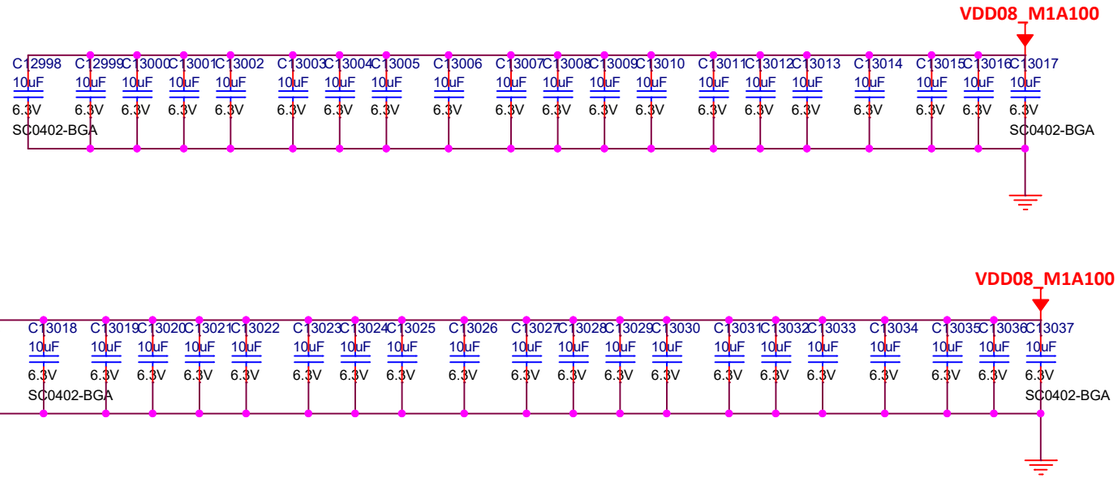
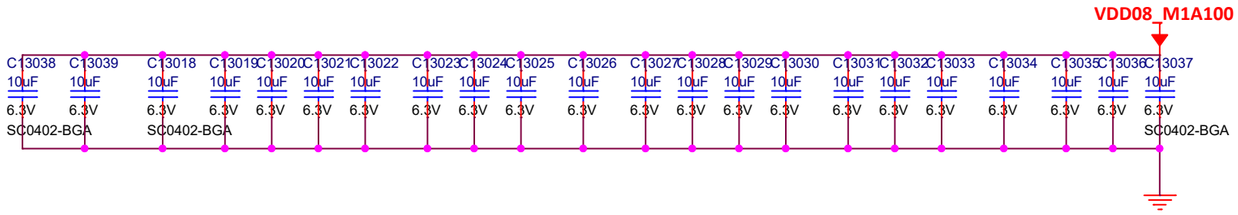
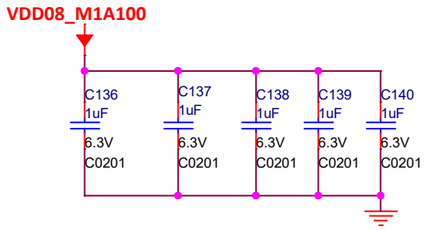
SOC-CPU Core







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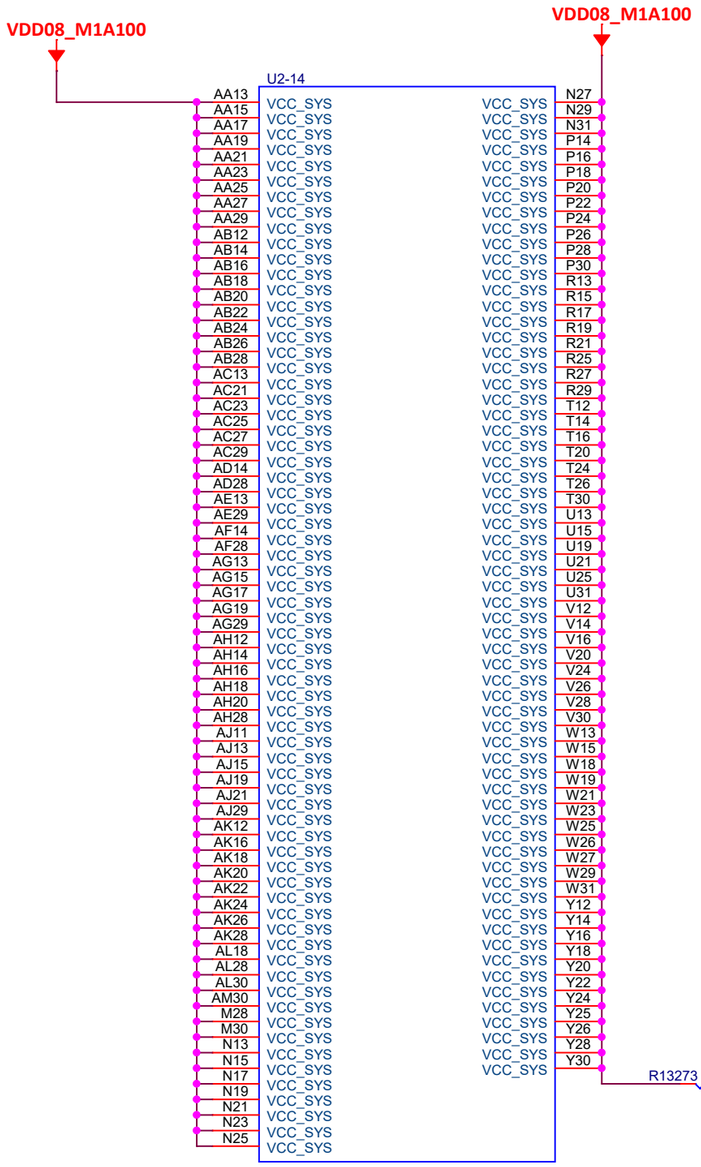

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SOC-0V8-PHY

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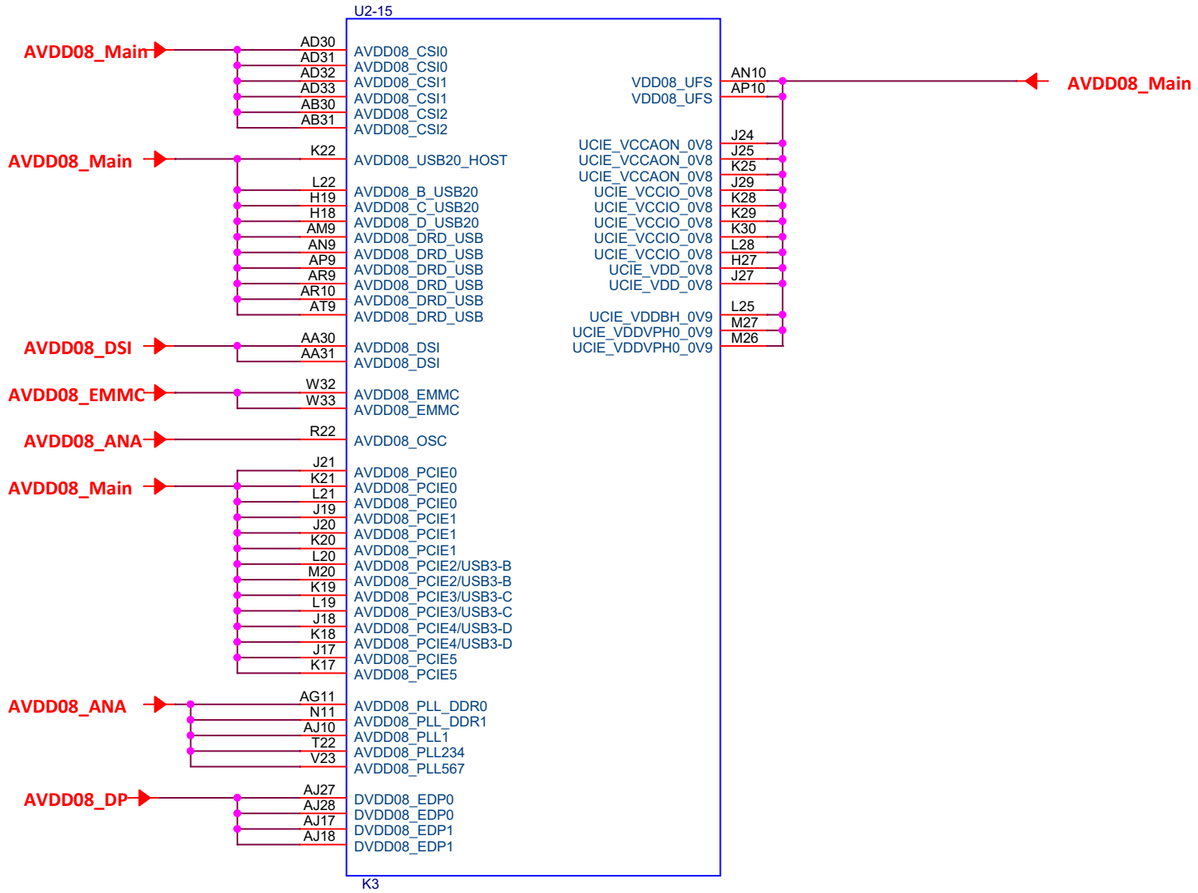

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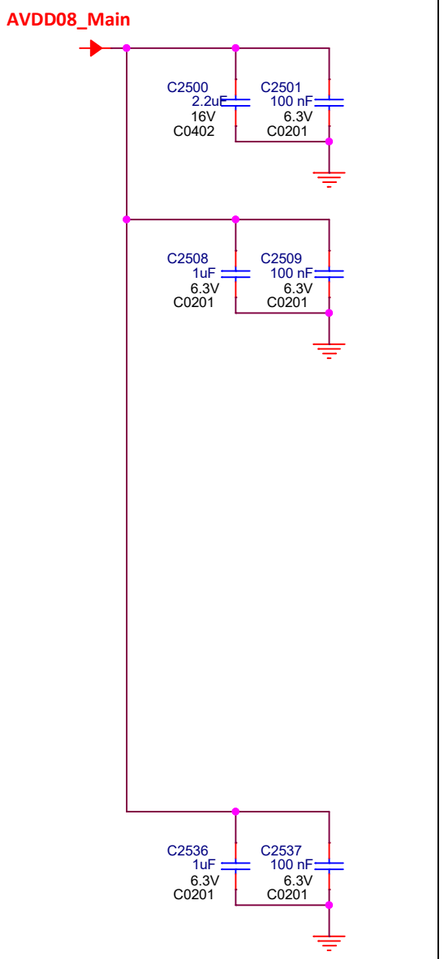
SOC-0V8-PHY CAP

USB20-PHY-CAP



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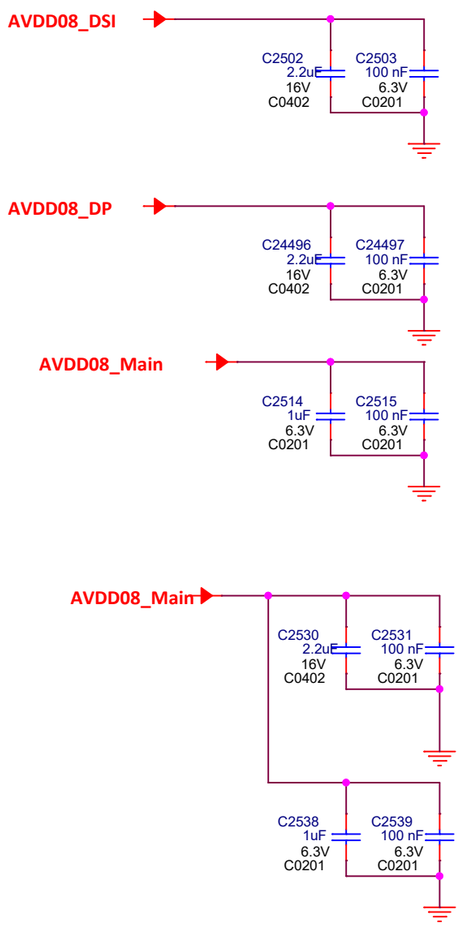

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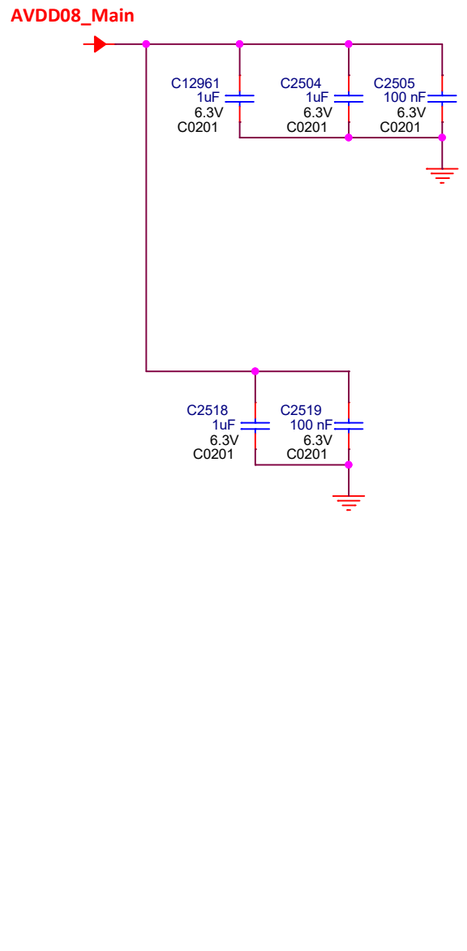
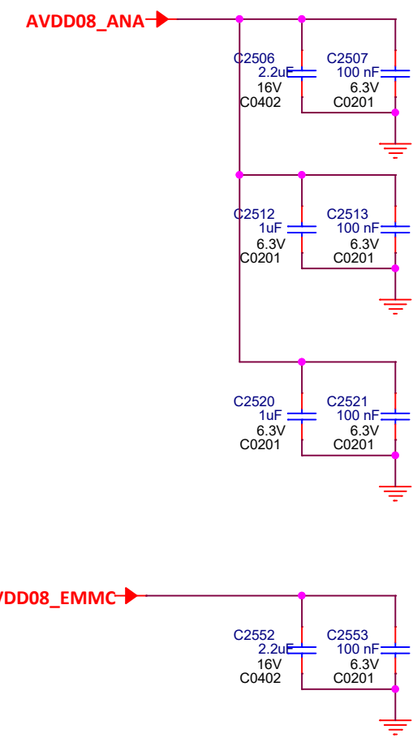


ANA-CAP



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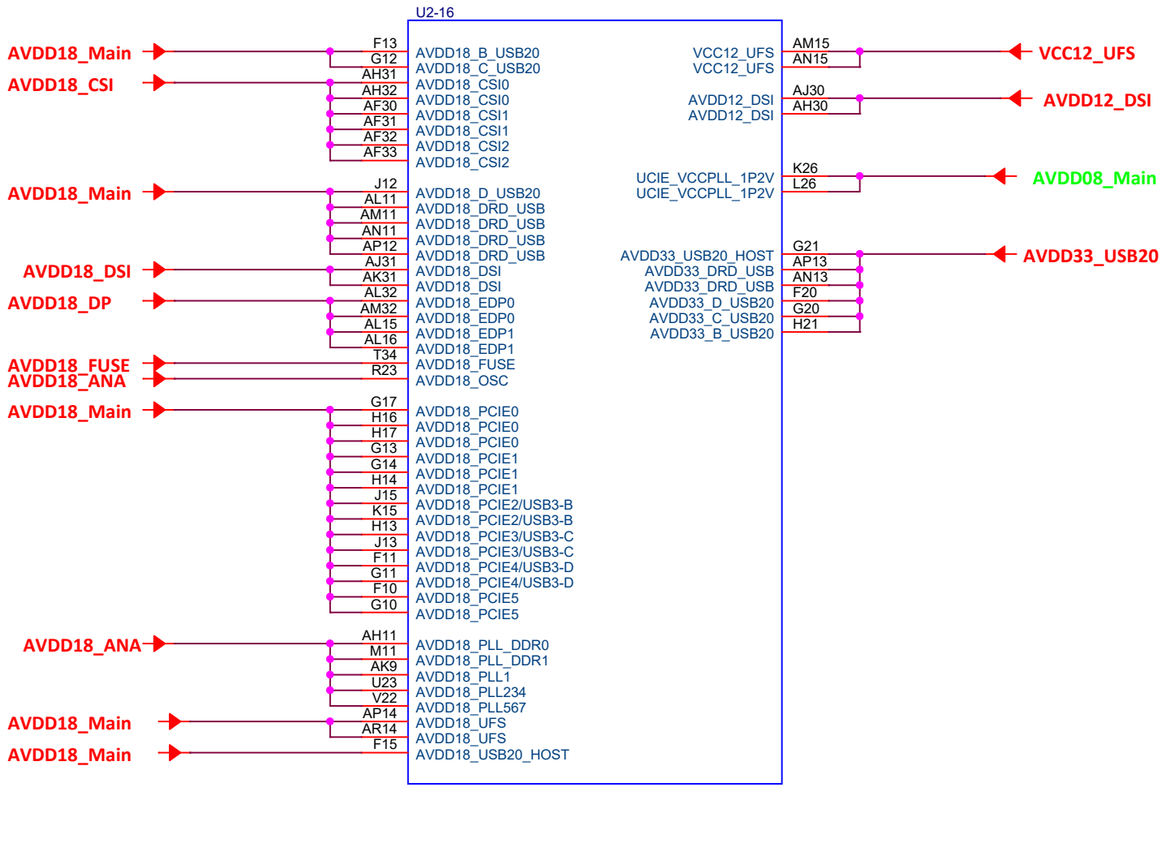
SOC-PHY PWR

VCC 0.8V ~~A~~phy CAP (next page)



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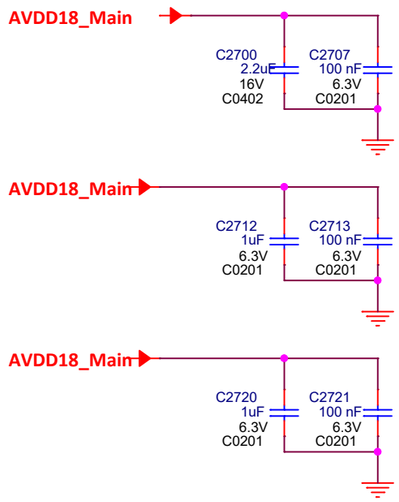
SOC-PWR CAP

USB20-PHY-1V8



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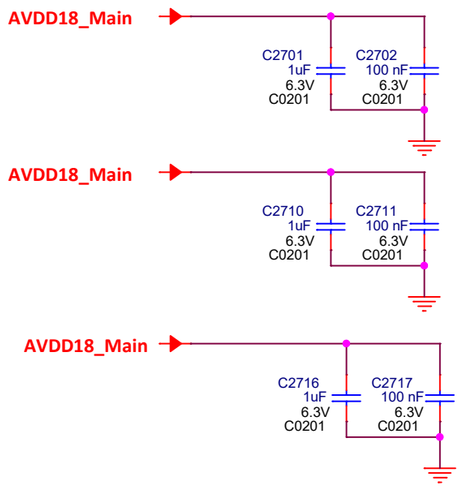

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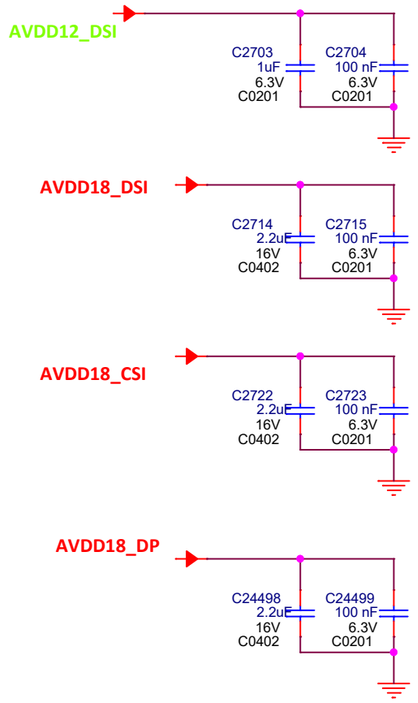

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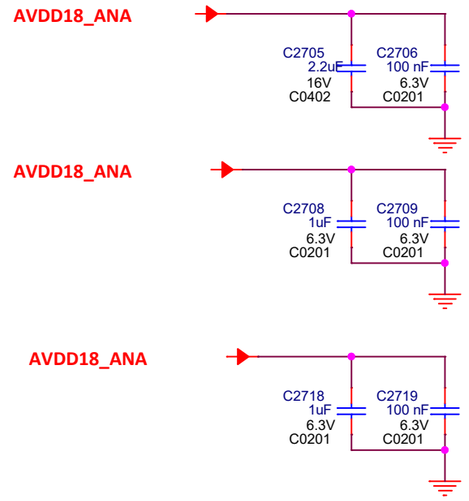

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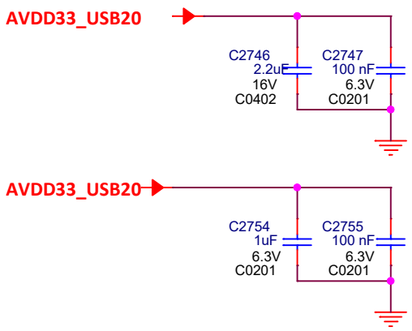

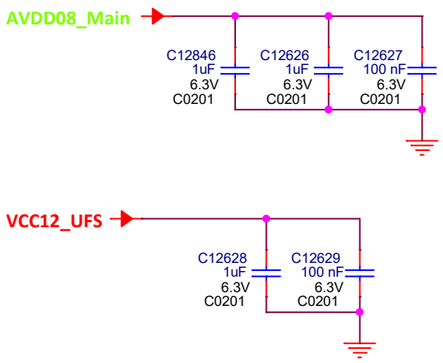

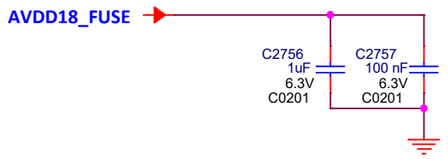

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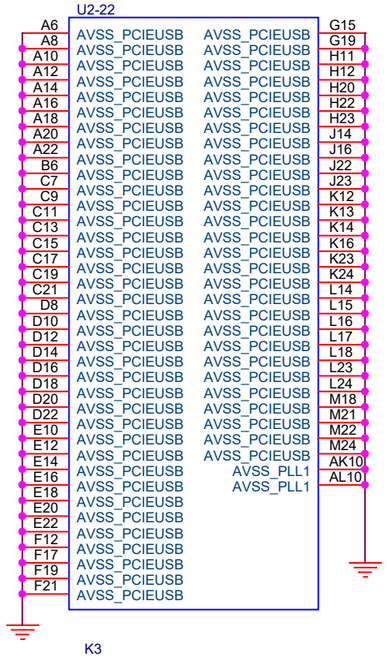

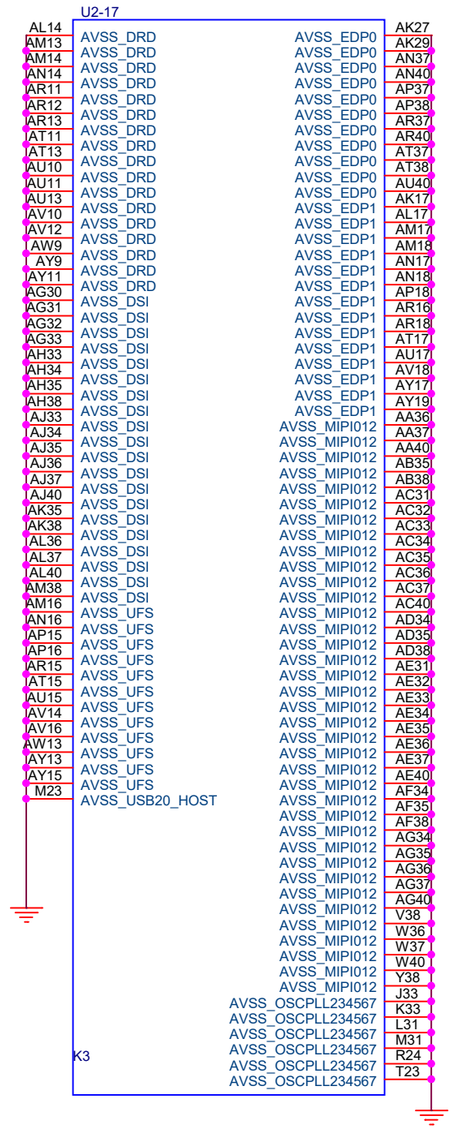

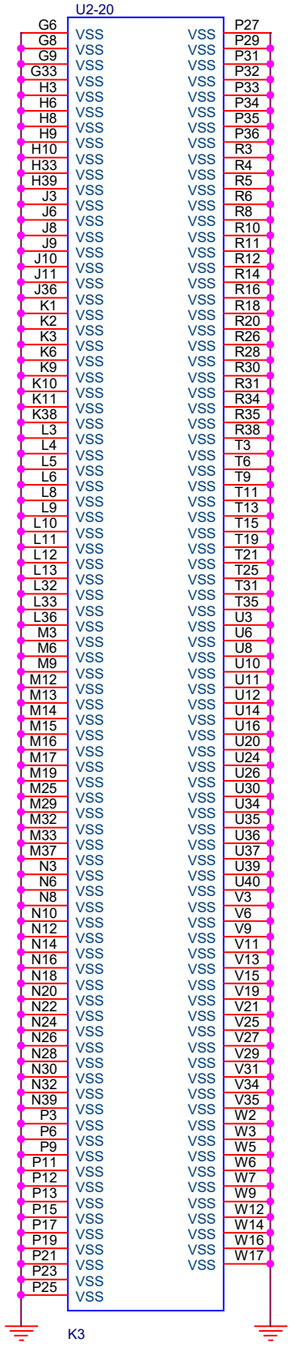

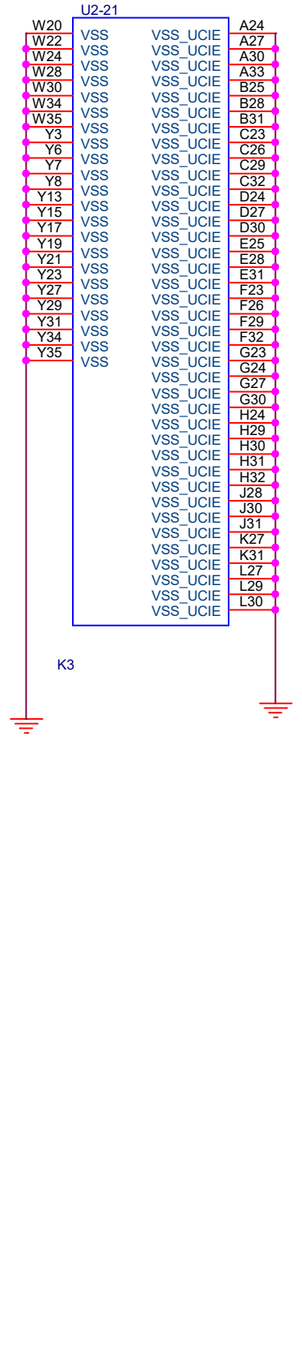

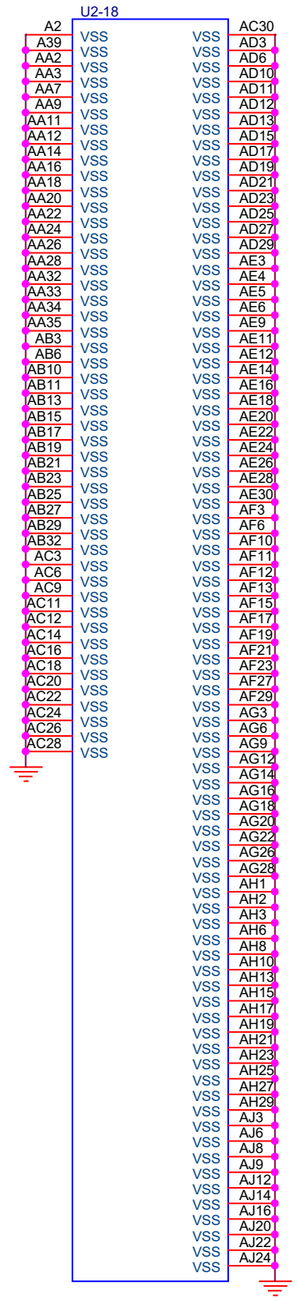

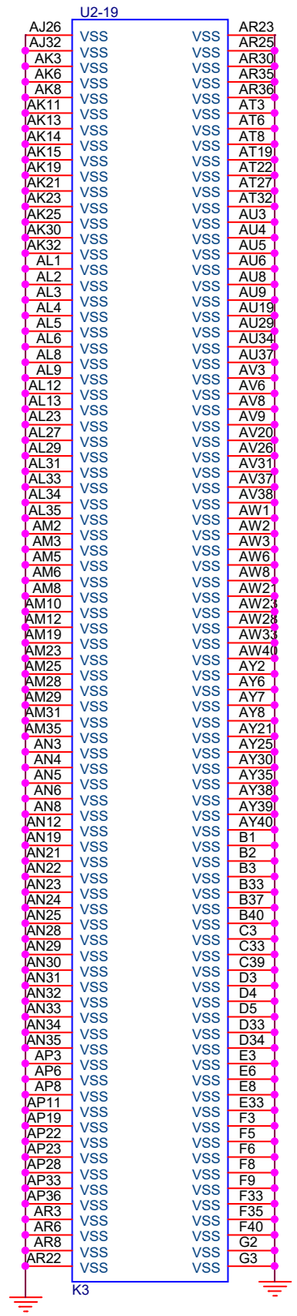

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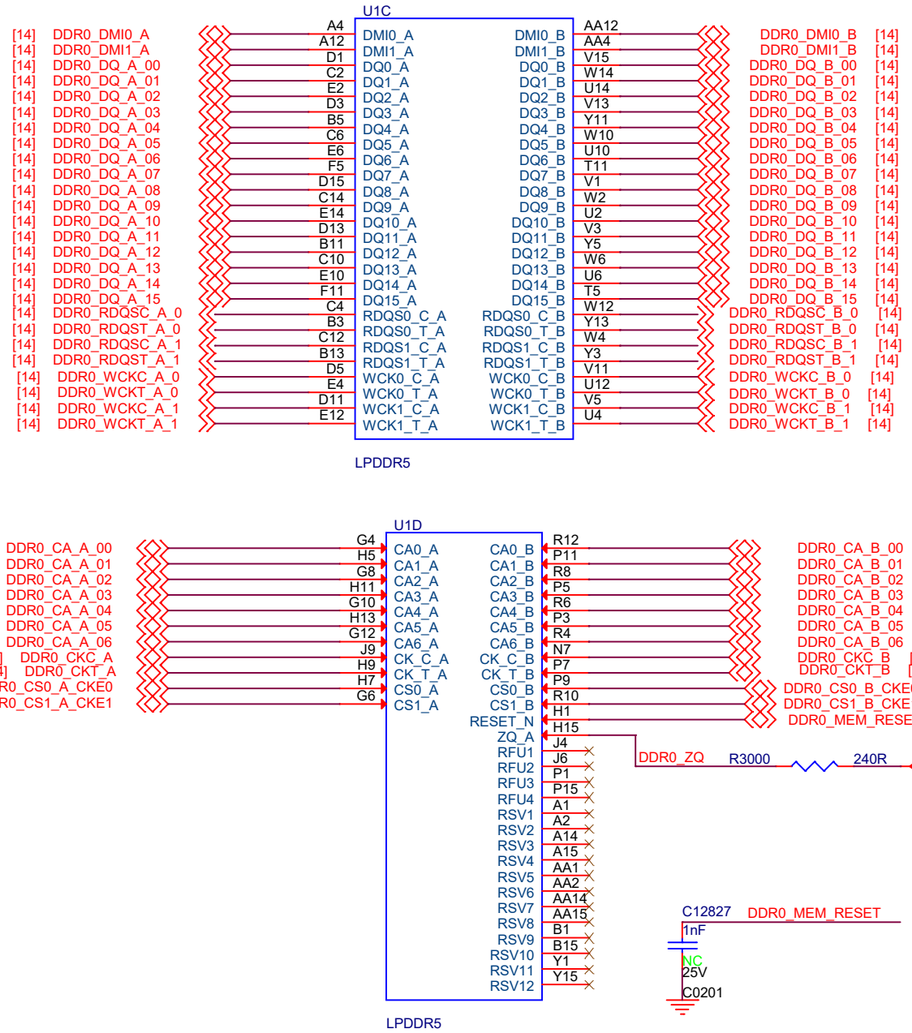
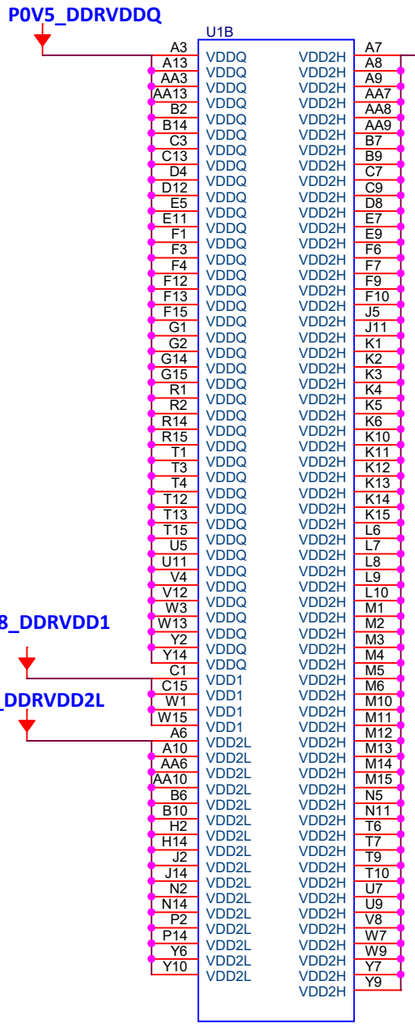
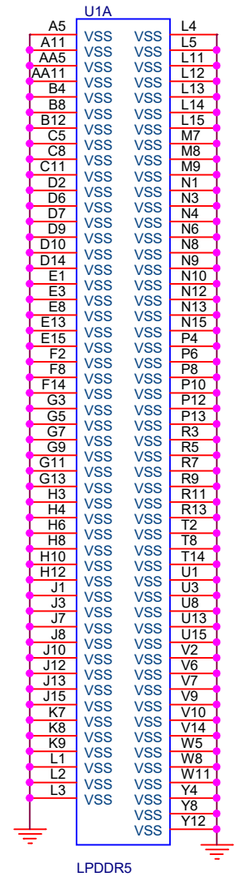
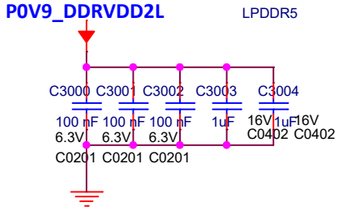
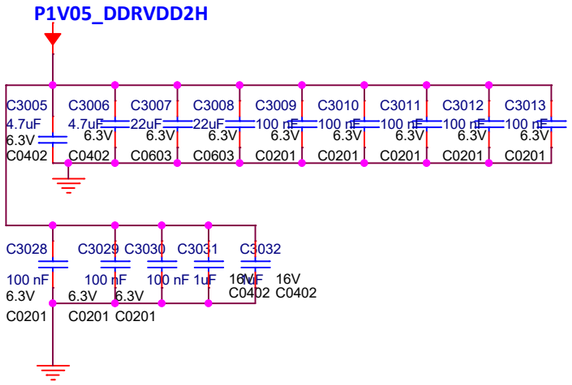
LPDDR5-0 SDRAM

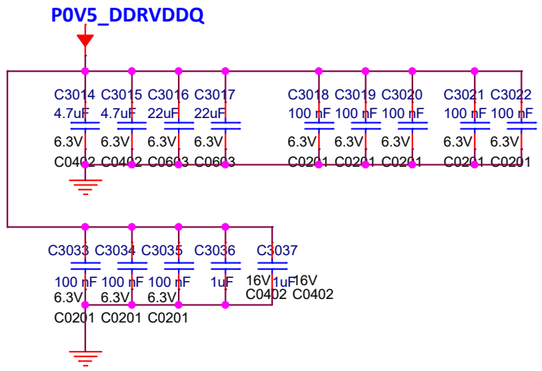


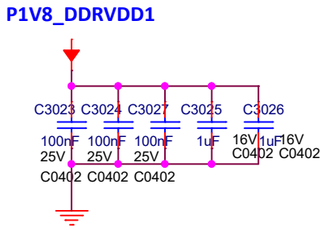












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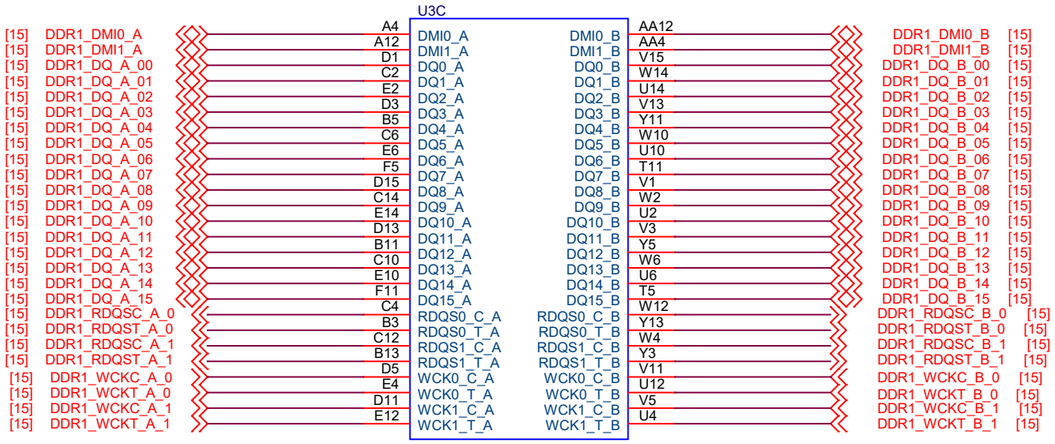
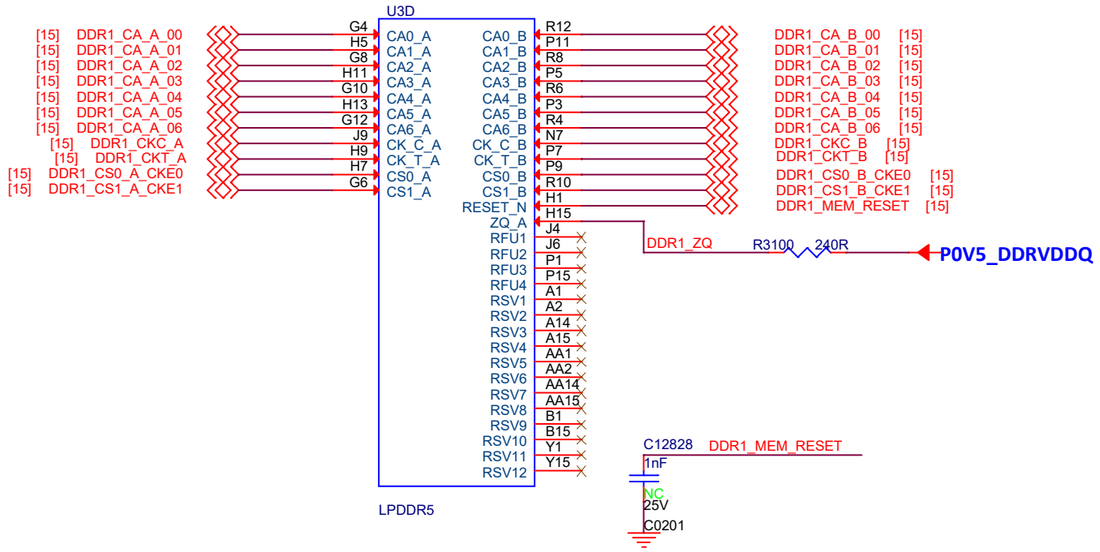
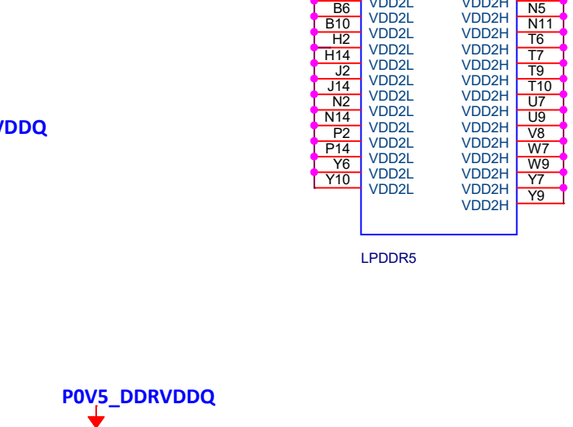
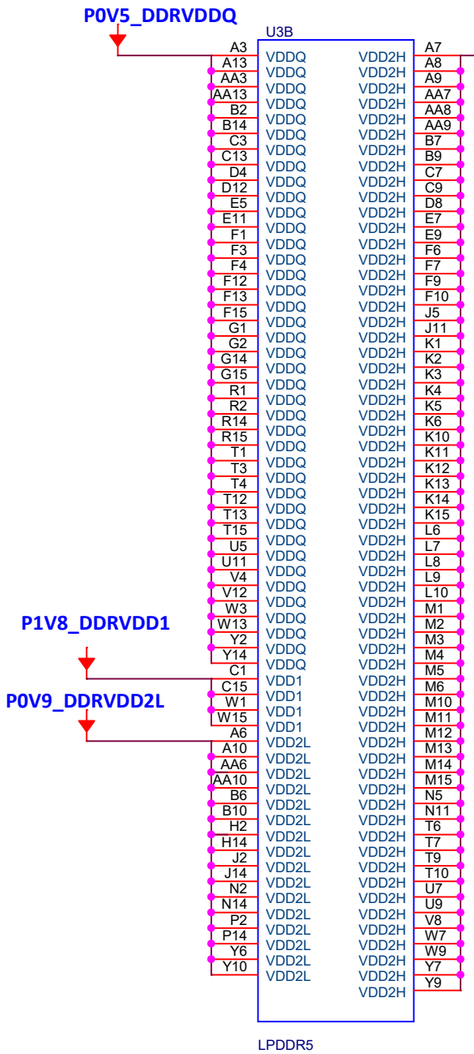
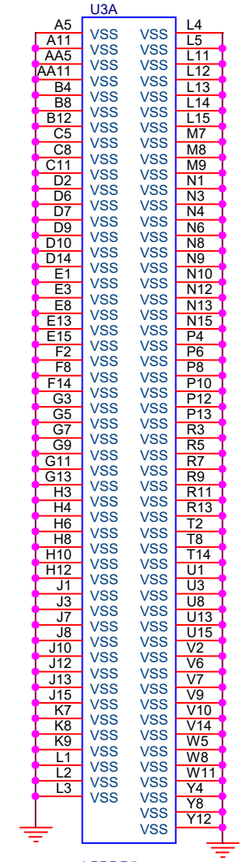
LPDDR5-1 lpddr5 颗粒

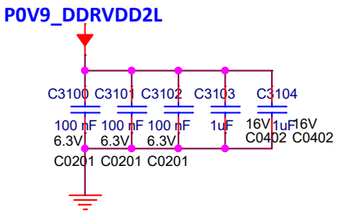


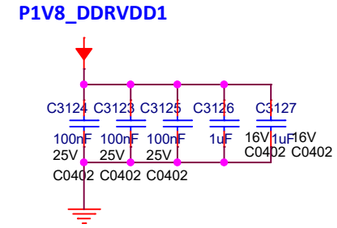












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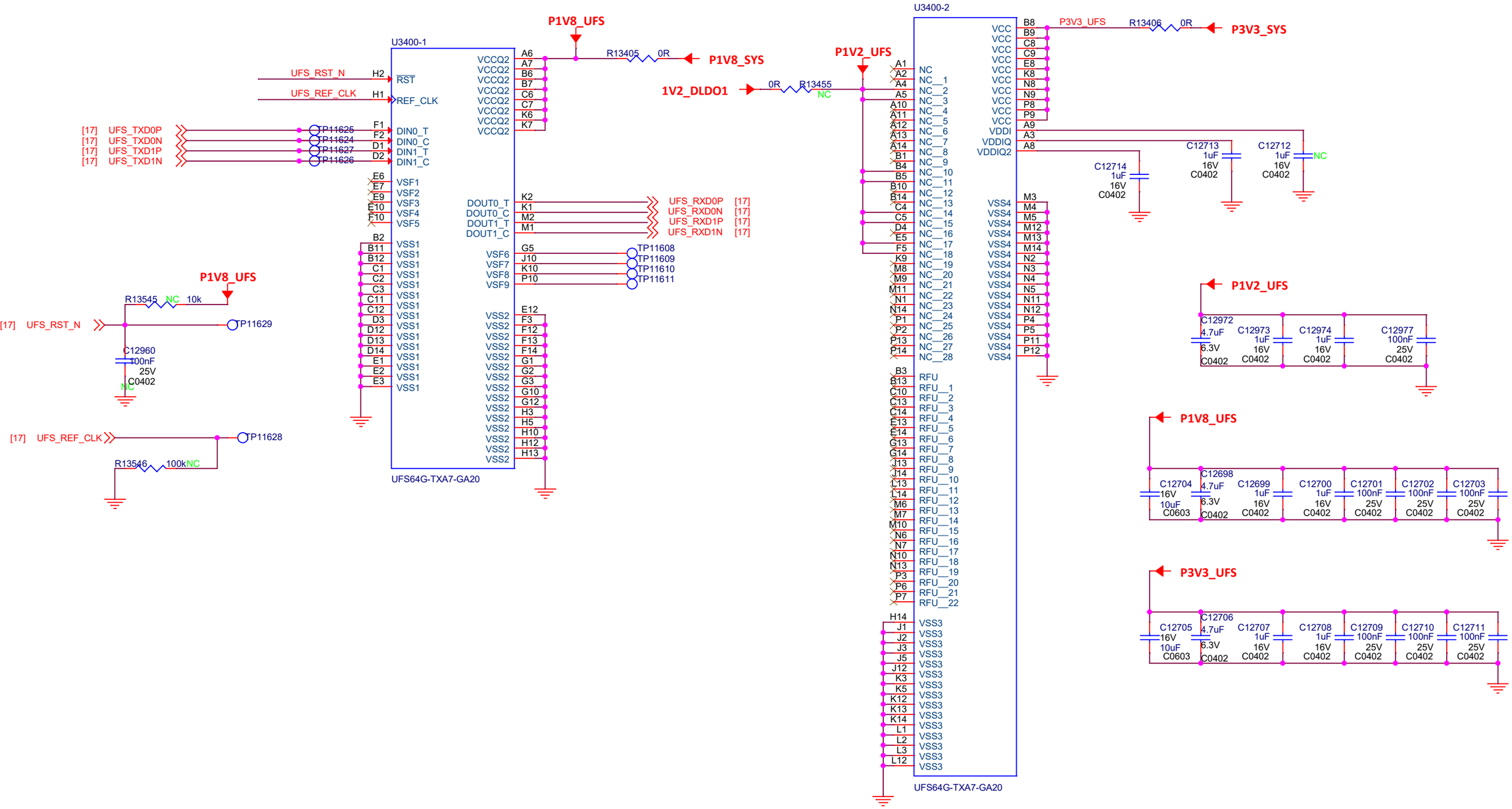
UFS



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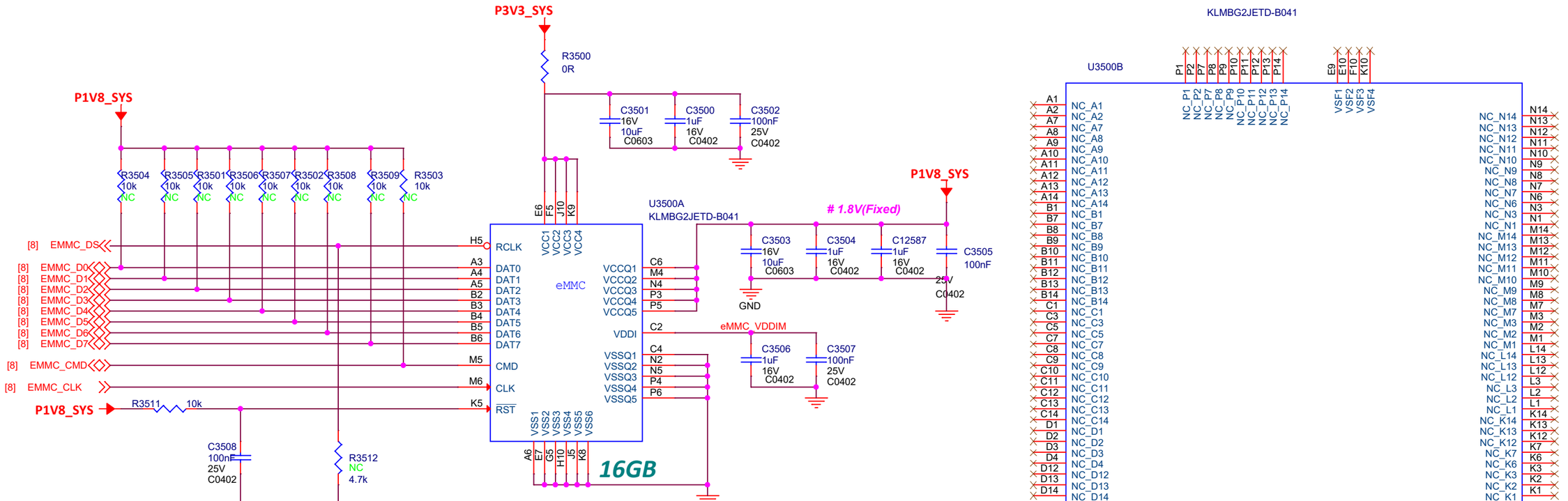
eMMC5.1



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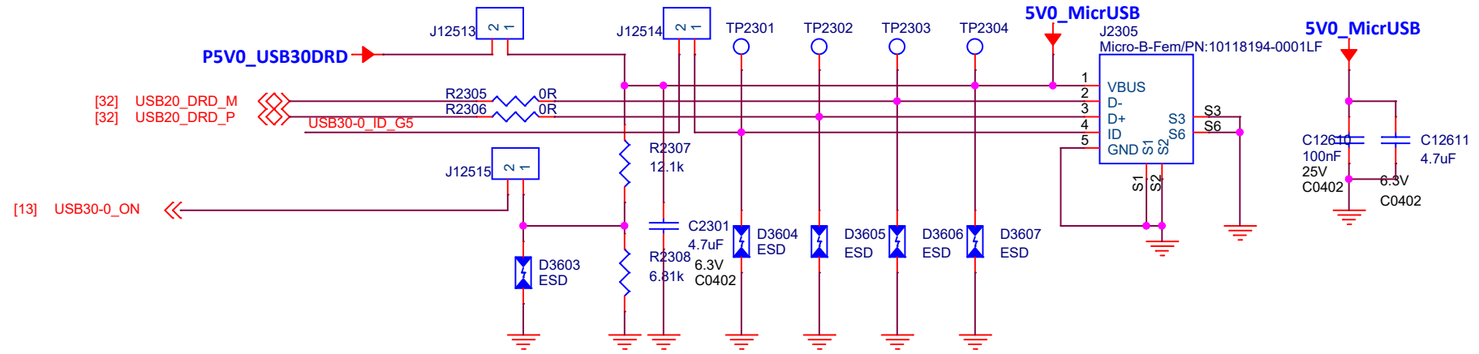
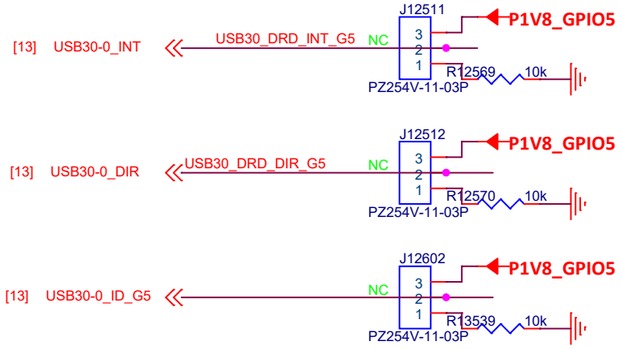
USB20 Mircro & TypeA

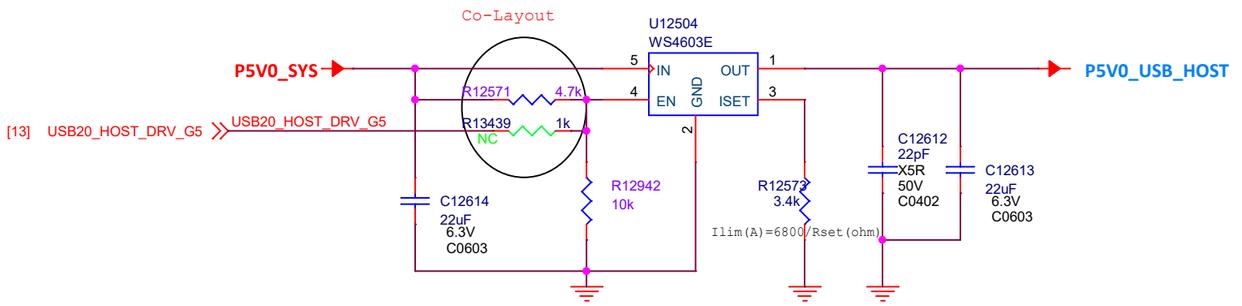
MICRO USB[DRD USB2.0 OTG]

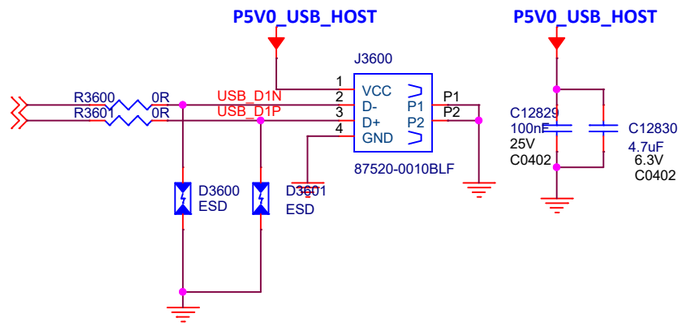
HW & SW: MicroB 验证USB30 DRD用
[without CC logic debug]





USB2.0 HOST PORT





1. K3 IO EN,需要把两个紫色电阻NC;
2. en vih 1.6V ,io en 略有风险;(非必要IO en操作, 验证芯片理论DRV 输出H即可)。
3. G5 io 可以切换IO 电压domain到3.3V

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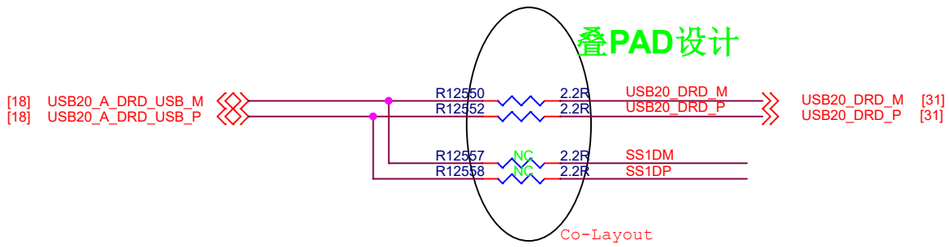
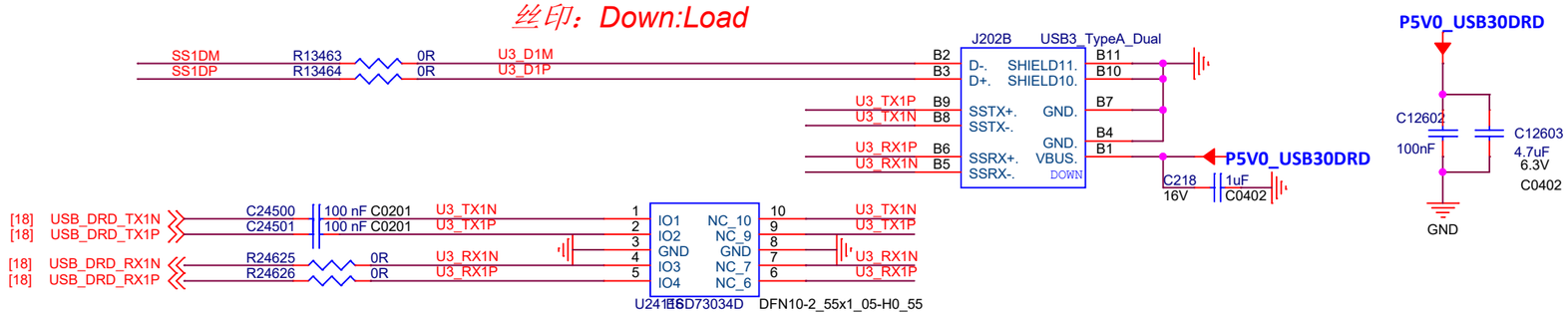
USB 3.0 DRD TypeA

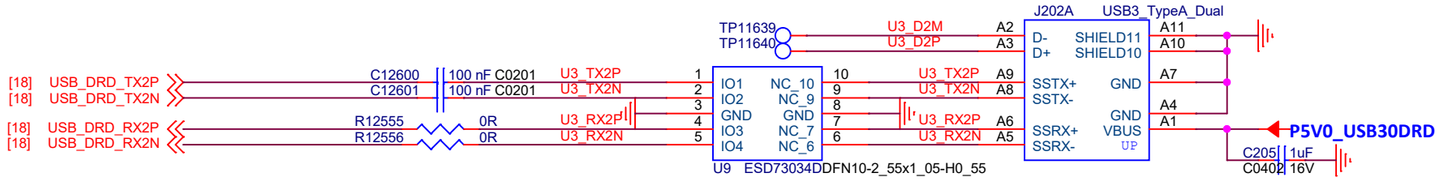
HW & SW: 两个TypeA 2选1应用,验证USB30 DRD用
[without CC logic debug]

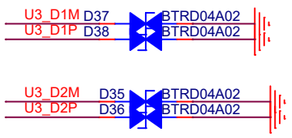


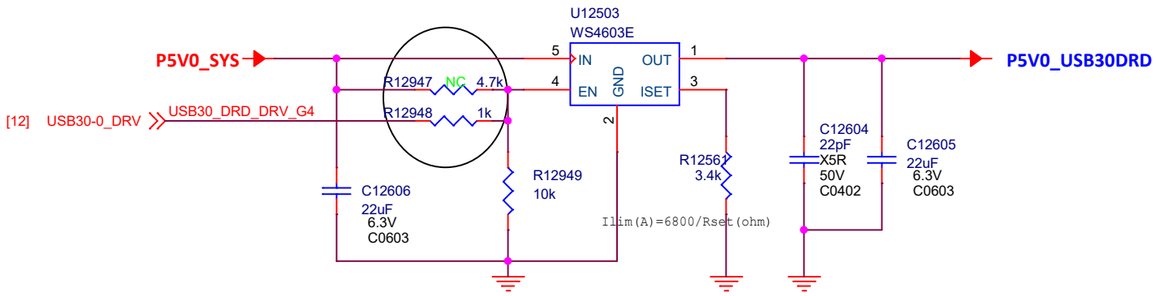
USB30 TypeA Connector

丝印：Down:Load









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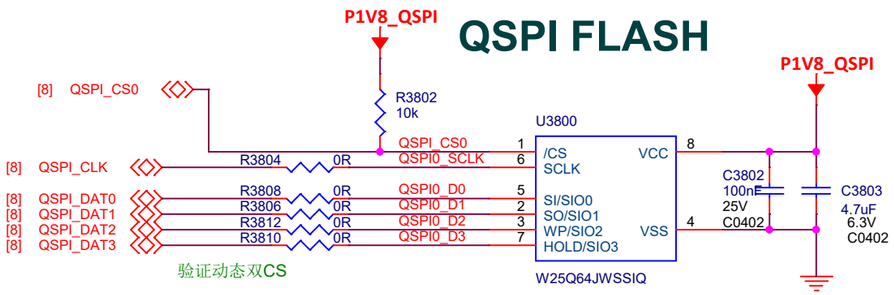
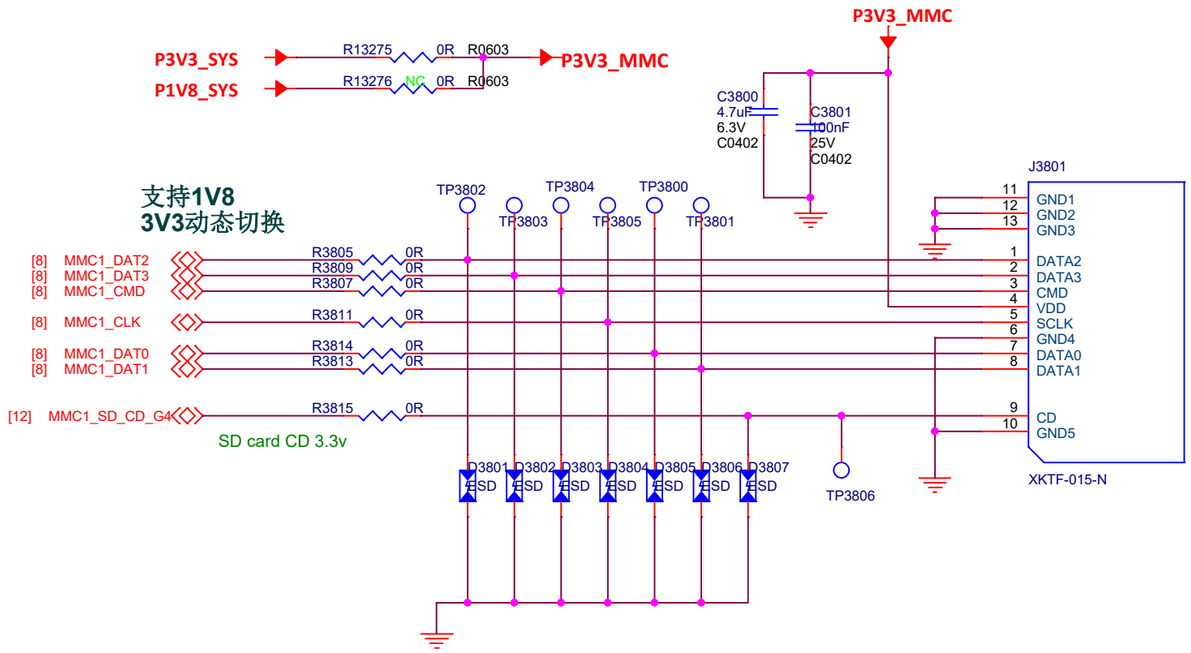
QSPI Flash & MMC

QSPI FLASH



Micro SD[MMC1]



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Debug Boot&Config&EEPROM

[11] Strap0_G3IO65
[11] Strap1_G3IO66
[11] Strap2_G3IO68
[11] Strap3_G3IO69

Strap0_G3IO65
Strap1_G3IO66
Strap2_G3IO68
Strap3_G3IO69

[11] Strap4_G3IO64
[11] Strap5_G3IO52

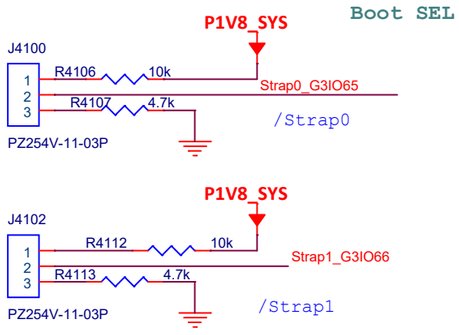
Strap4_G3IO64
Strap5_G3IO52

Boot

bit(strp)3	bit(strp)2	bit(strp)1-0	bootmode
1	0	XX	Update from USB
1	1	XX	Update from Uart
0	X	10	Normal Boot From SPI Nand
0	X	01	Normal Boot From SPI Nor
0	X	00	Normal Boot From eMMC
0	X	11	Normal Boot From UFS

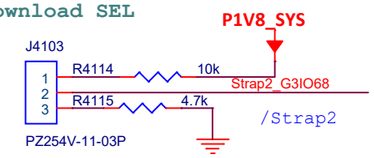
Boot

Boot SEL



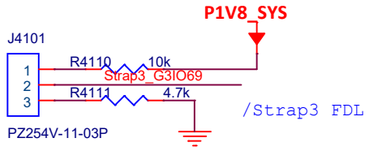
Strap1	Strap0	Function
0	0	TF Card -> EMMC
0	1	TF Card -> SPI NOR
1	0	TF Card -> SPI NAND
1	1	TF Card -> UFS

Download SEL



Strap2	Function
0	USB
1	UART

Boot/Download SEL

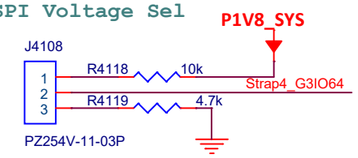


FDL	Function
0	启动
1	下载

QSPI/LPDDR config

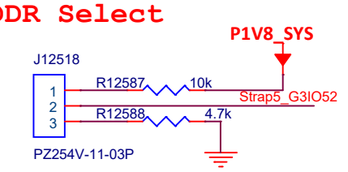
内部集成PRI JTAG/ SEC JTAG
Sec_JTAG 只访问RCPU 不需要JTAG SEL

QSPI Voltage Sel



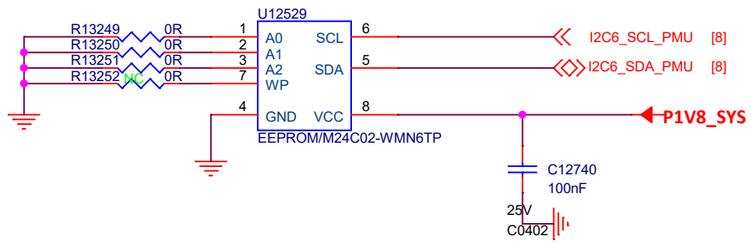
GPIO	Function
0	3V3
1	1V8

DDR Select



GPIO	Function
0	LPDDR5
1	LPDDR4x

EEPROM



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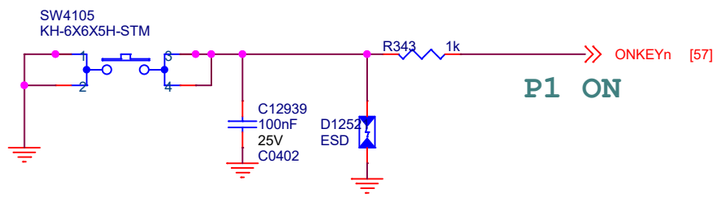
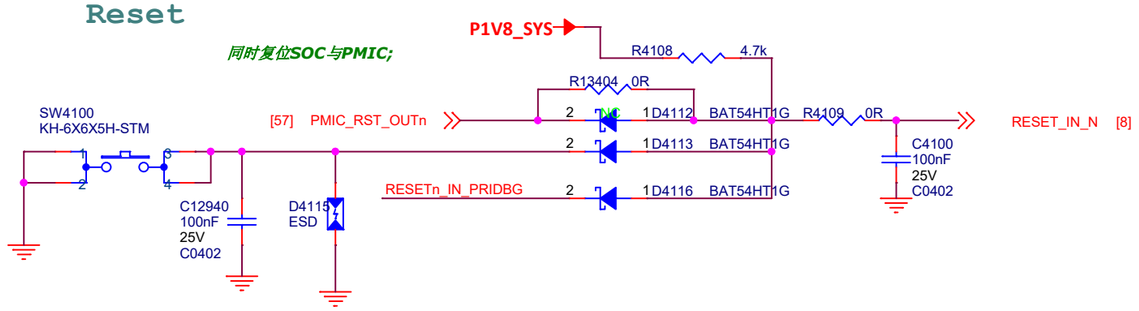
config

PWR ON

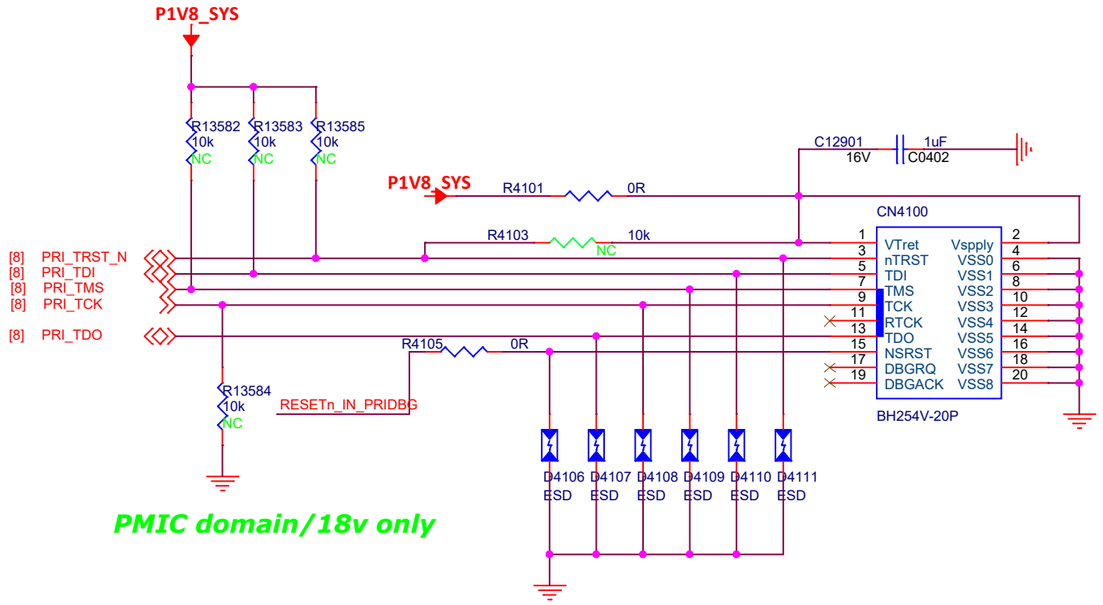


P1 ON

Reset

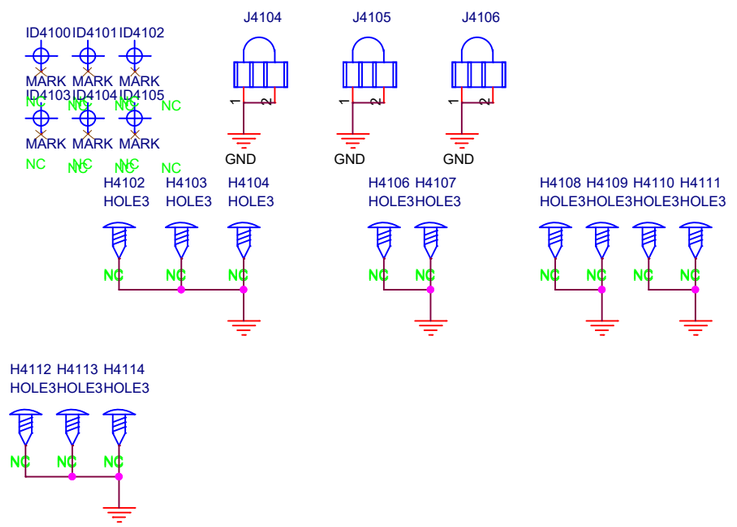


PRI JTAG



PMIC domain/18v only

Hole



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PDN -0V8 CPU/Core

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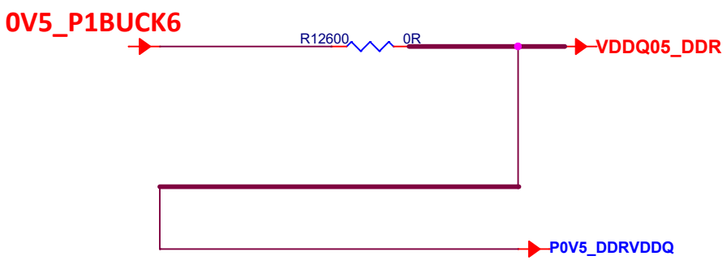
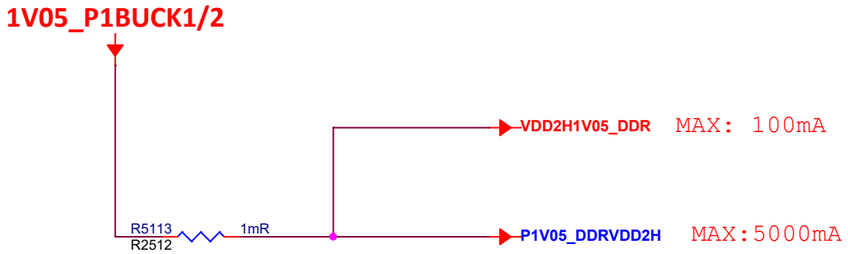
PDN LPDDR5-1/2





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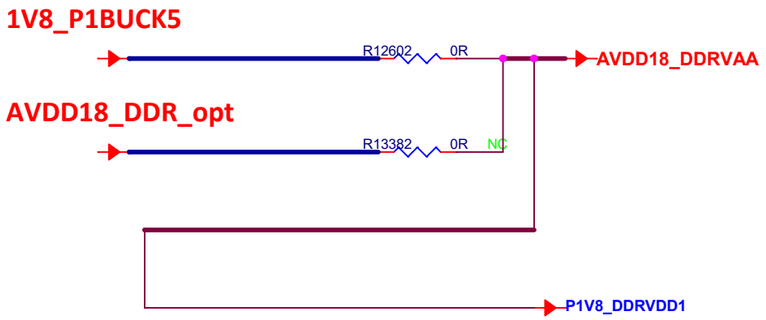
PDN LPDDR5



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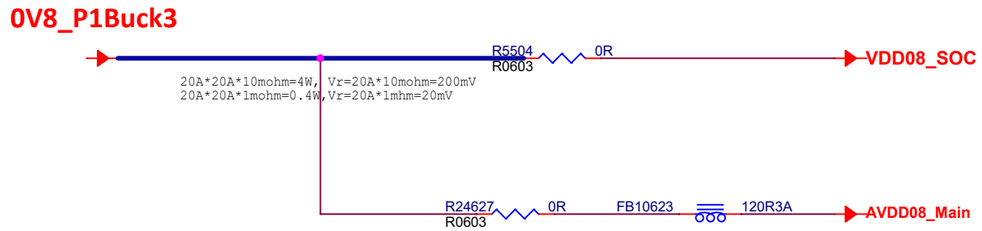
PDN -0V8 SOC Main path 1/3



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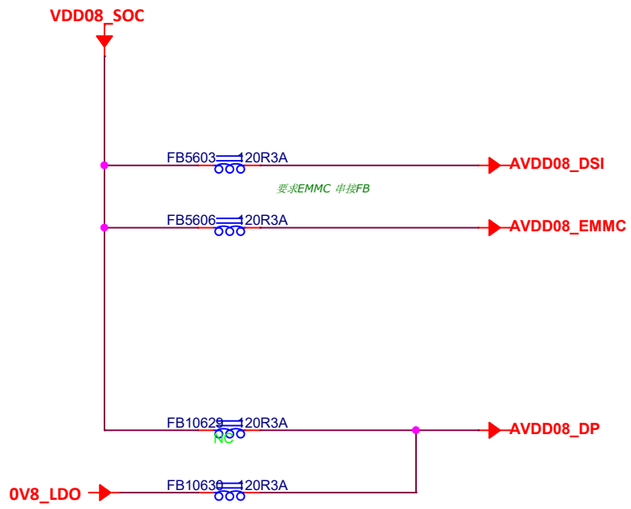
PDN -0V8 SOC Branch 2/3

Sub Path



1A*A*10mohm=10mW, Vr=1A*10mohm=10mV

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PDN -0V8 SOC Branch 3/3

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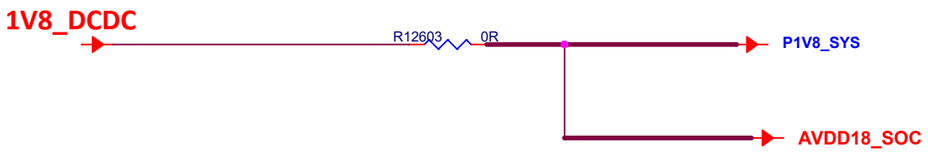
PDN - 1V8 SOC Main path



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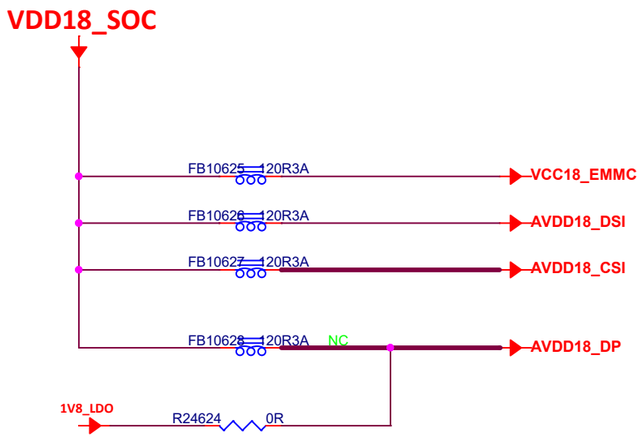
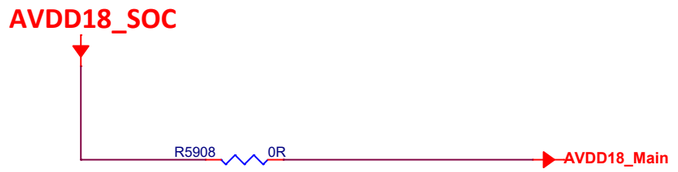
PDN - 1V8 Sub path

VDD18 [P1 LDO source] Sub path



AVDD18 [DCDC source] Sub path



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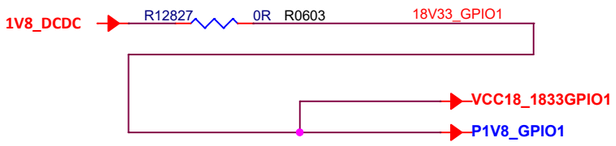
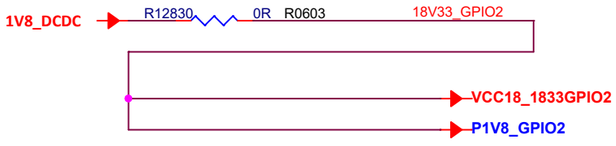
PDN - 1833-GPIO& QSPI

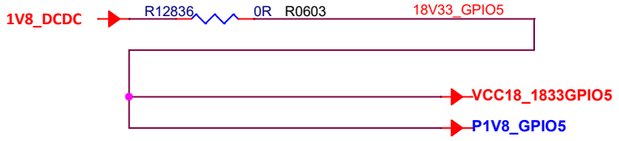
DET

当个别EVB需切换3.3V 测试，
断开1833电阻，杜邦线到排针

（使用杜邦线识别板子IO以及防止误触）







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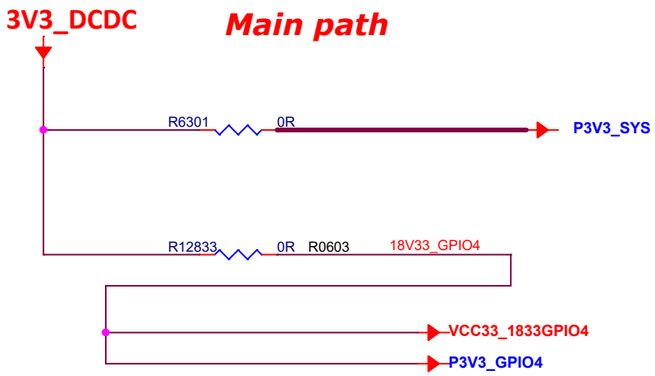
PDN -3V3 GPIO4



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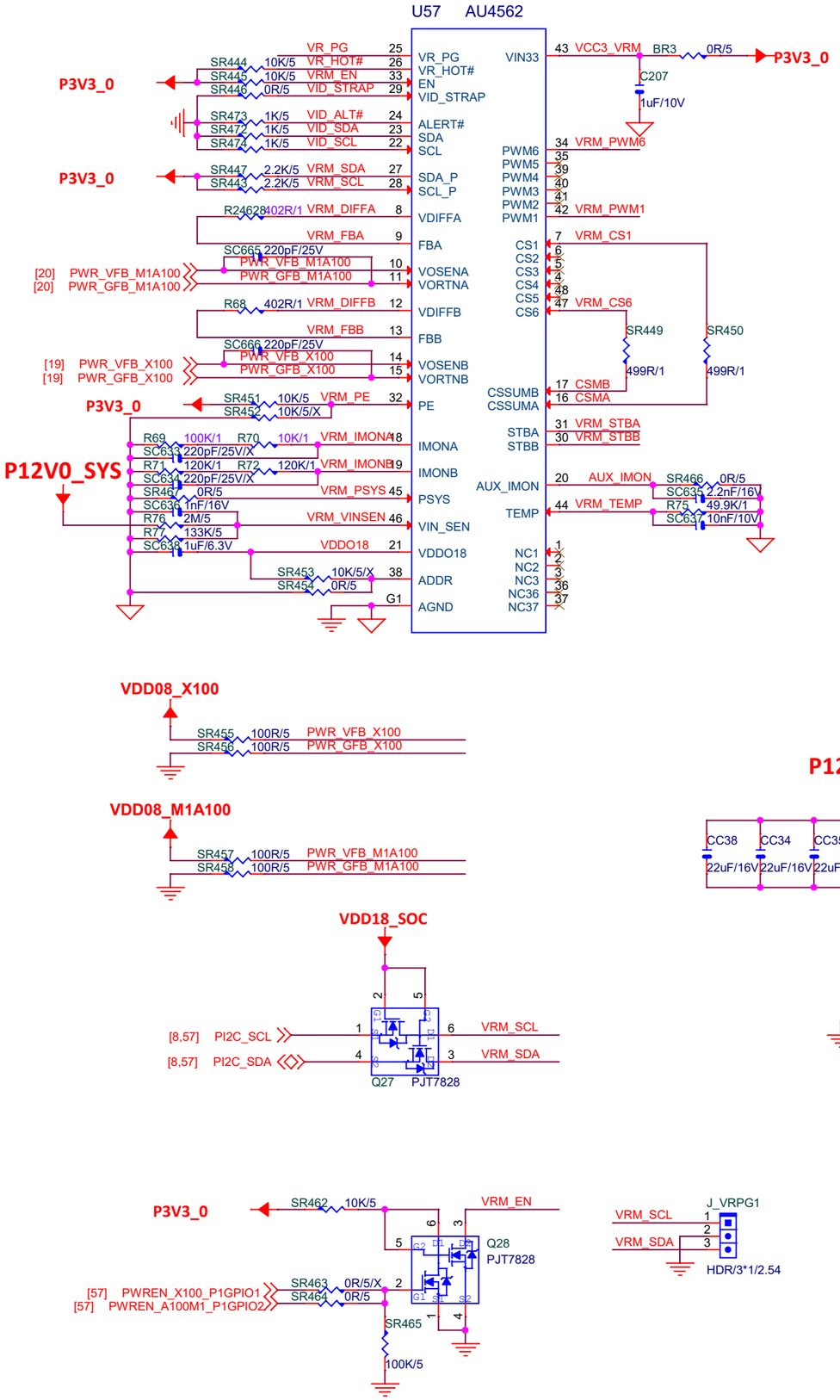
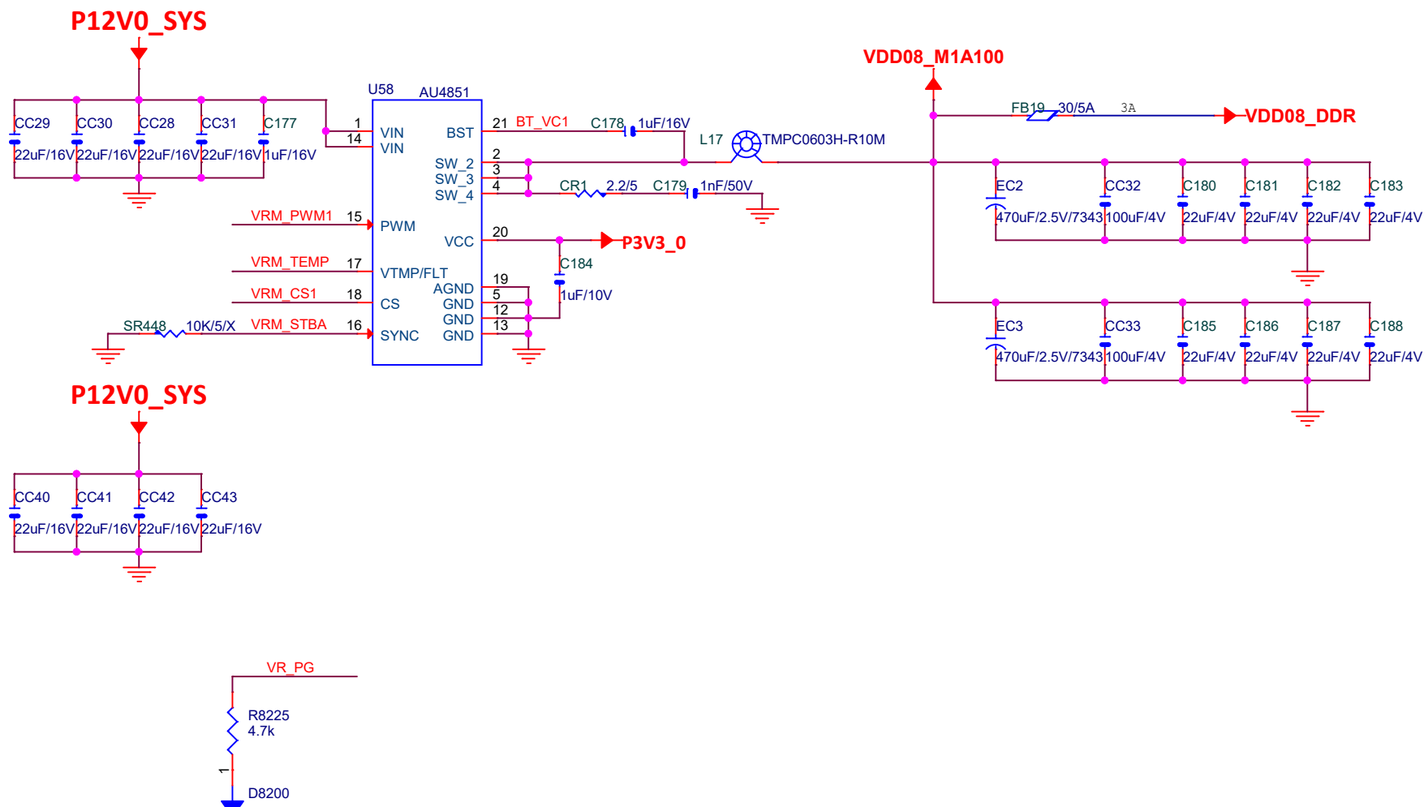
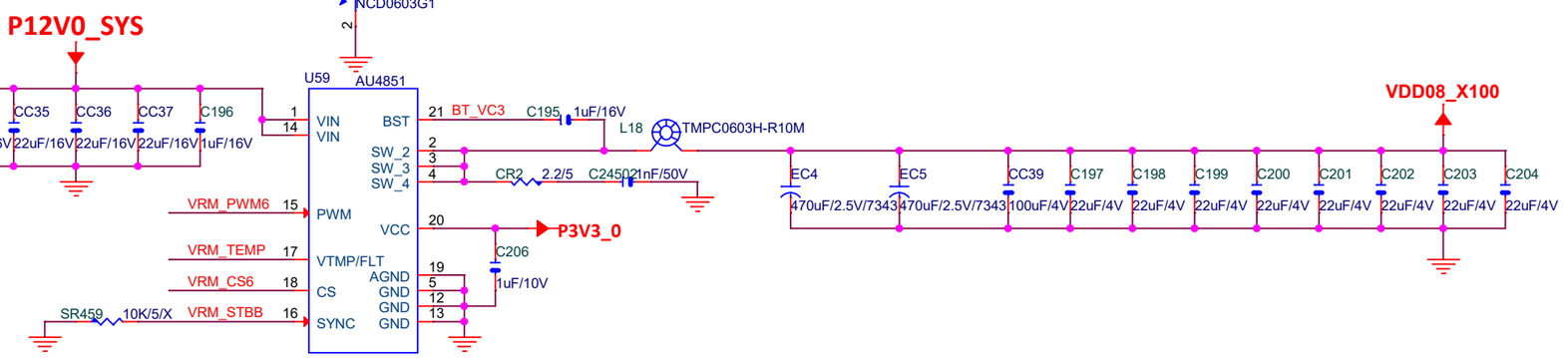
Power - VR-CPU







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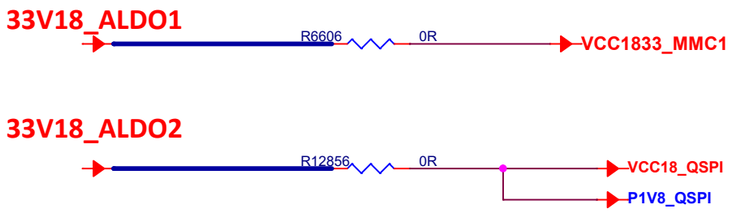
PDN -ALDO



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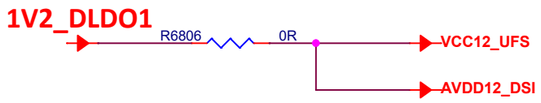
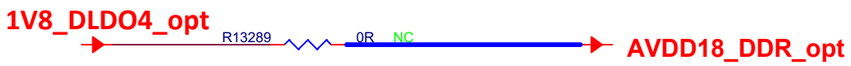
PDN -DLDO1-4





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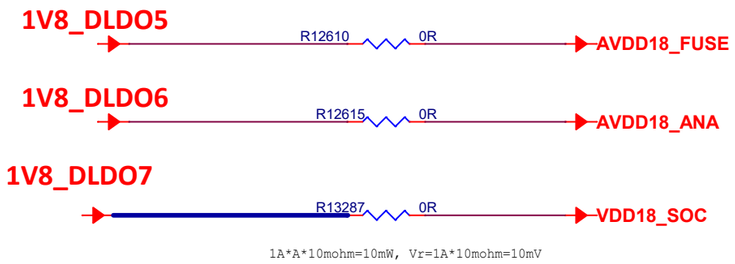
PDN -DLDO 5-7



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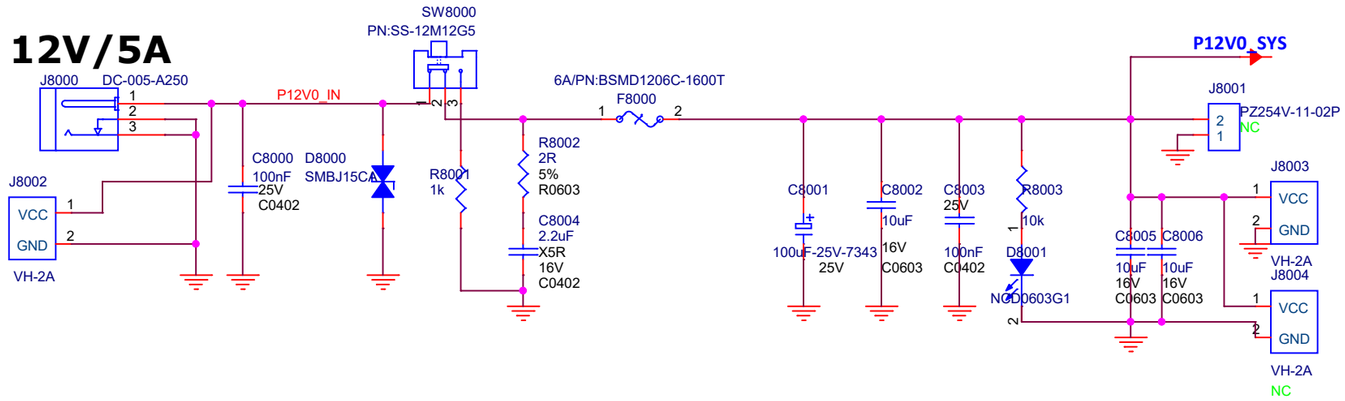
12V DC IN



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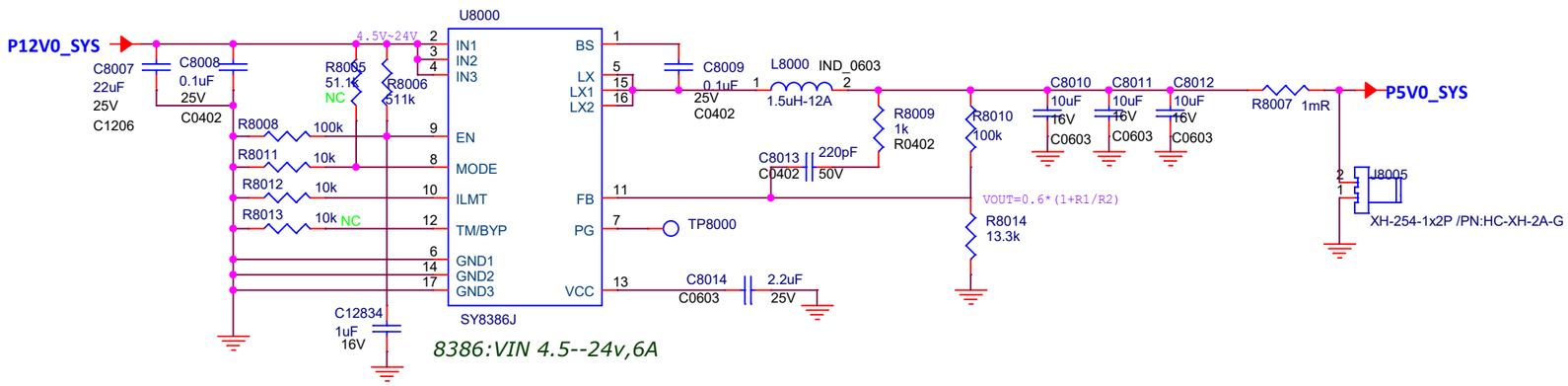

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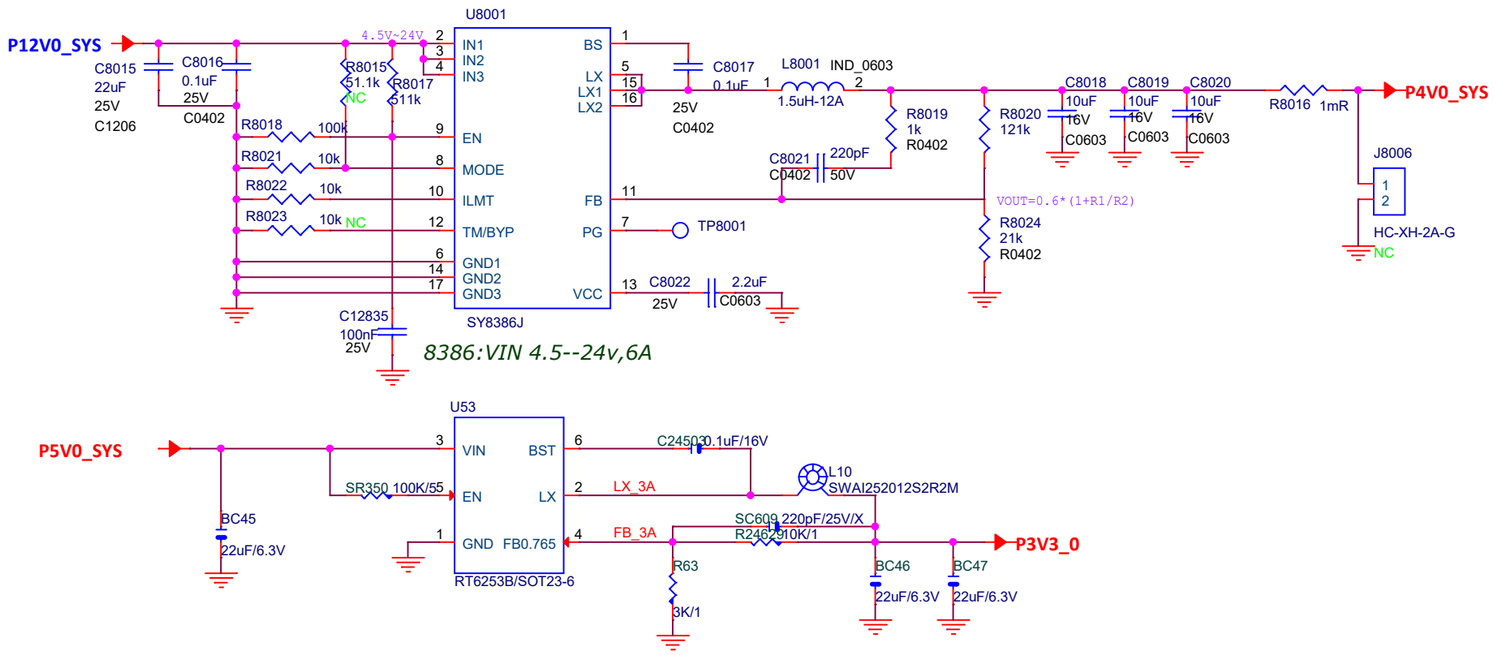

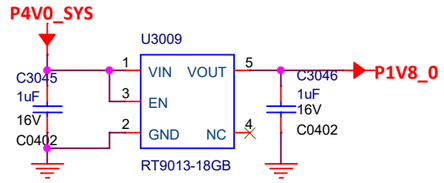

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LPDDR5 DCDC

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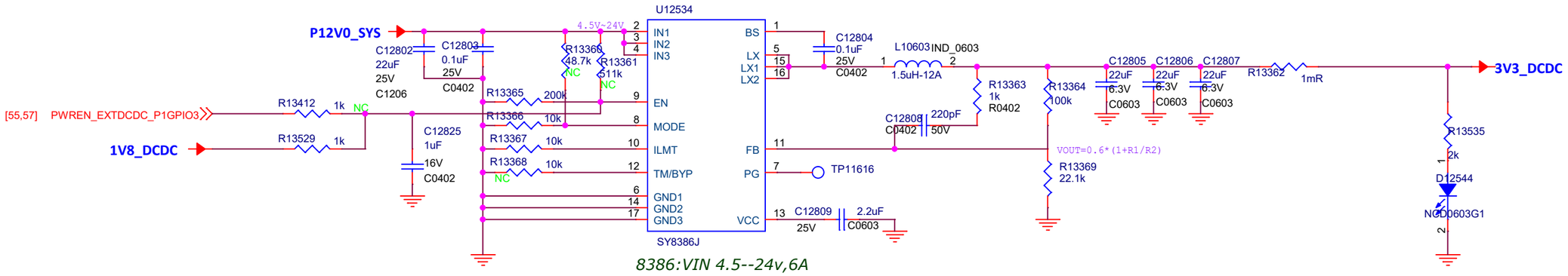
3V3_DCDC



8386:VIN 4.5--24v,6A

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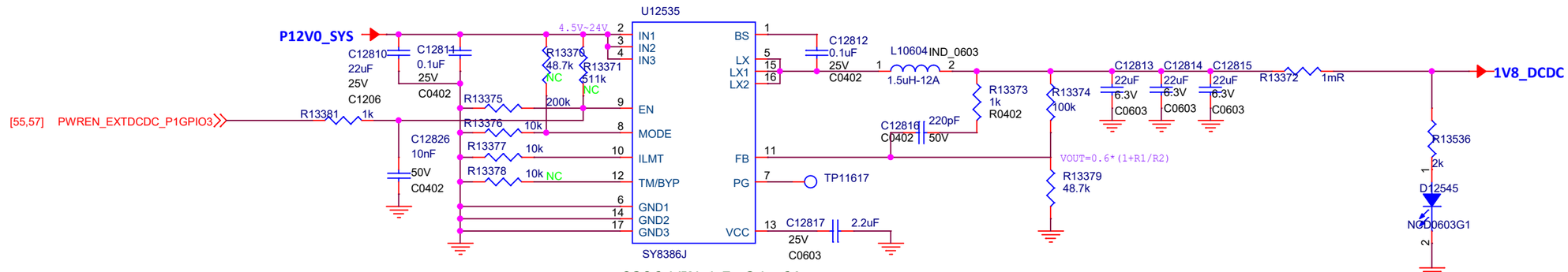

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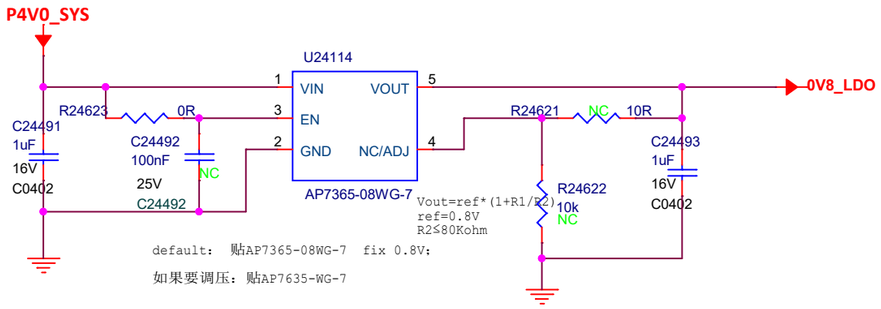

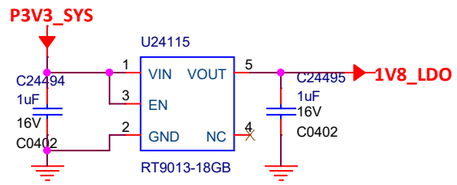

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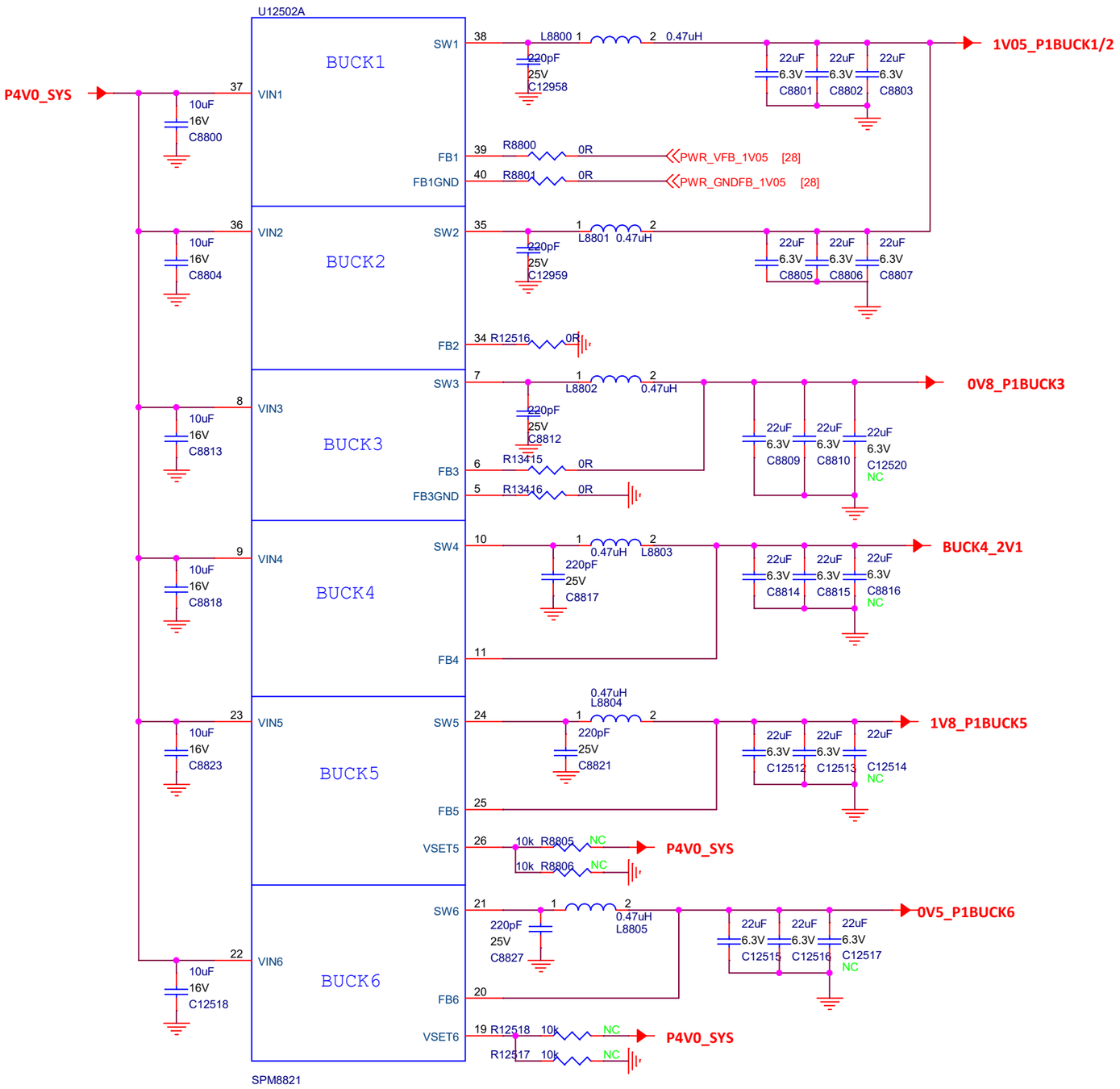
PMIC 1/2 BUCK



BUCK1 BUCK2	1V05_P1BUCK1/2	VDD2H1V05_DDR P1V05_DDRVDD2H[MAX5A]
BUCK3	0V8_P1BUCK3	VDD08_SOC 0V8_DDR(opt)
BUCK4	**BUCK4_2V1**	
BUCK5	1V8_P1BUCK5	AVDD18_DDRVAA P1V8_DDRVDD1
BUCK6	0V5_P1BUCK6 [DCDC 0.3V opt]	VDDQ05_DDR P0V5_DDRVDDQ

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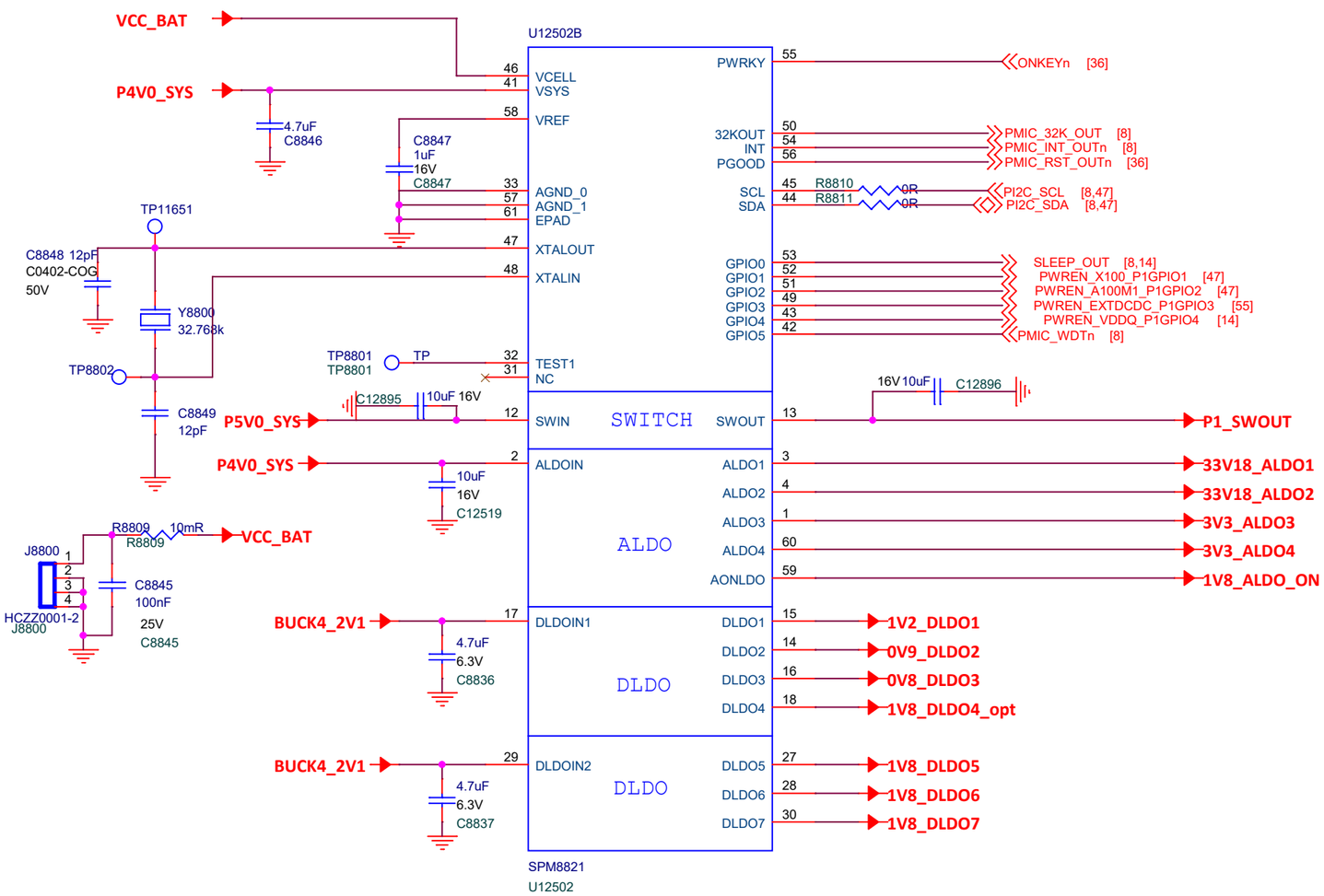
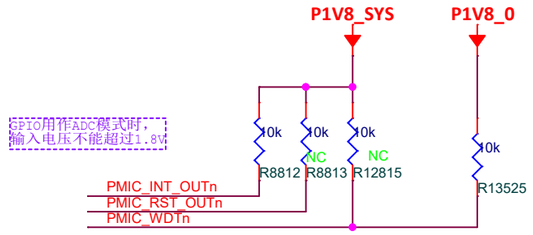
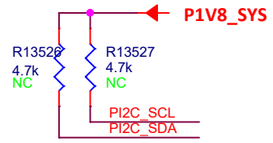
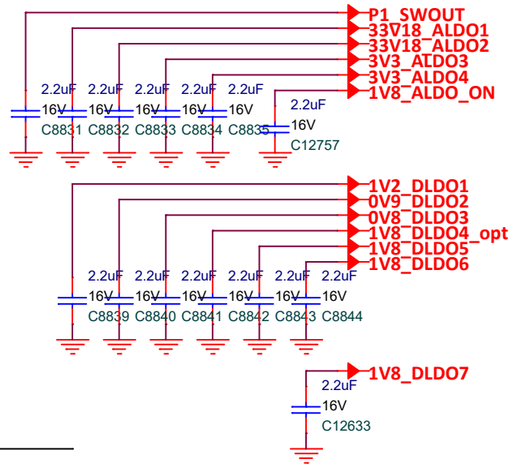
PMIC 2/2 LDO & Contr









33V18_ALDO1	VCC1833_MMC1
33V18_ALDO2	VCC18_QSPI P1V8_QSPI
3V3_ALDO3	P3V3_CAM
33V18_ALDO4	AVDD3V3_USB
ALDO ON	P1V8_opt

1V2_DLDO1	AVDD12_SOC UFS_opt（1v2颗粒）
0V9_DLDO2	UCIE_VDDPBH_0V9 P0V9_DDRVDD2L
0V8_DLDO3	AVDD08_PLL
1V8_DLDO4_opt	AVDD18_DDR_opt[default] 2V8_DLDO4_opt

1V8_DLDO5	AVDD18_FUSE
1V8_DLDO6	AVDD18_PLL
1V8_DLDO7	VDD18_SOC

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