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Key Stone®

K1 Hardware Design Guide

V1.2 - 2026.09.04

Revision history



Version	Date	Notes
V1.2	2026.09.04	Updated the P1 switch capacitor labeling and the related picture in Section 1.1.4 Updated Preface
V1.1	2025.08.04	Added a note regarding GPIO90 when not in use
V1.0	2024.03.12	Initial release

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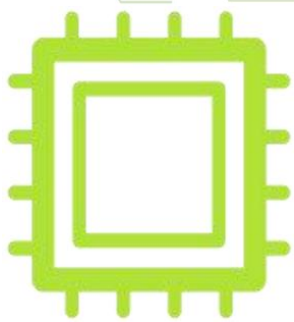
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Chapter 1

Schematic Design

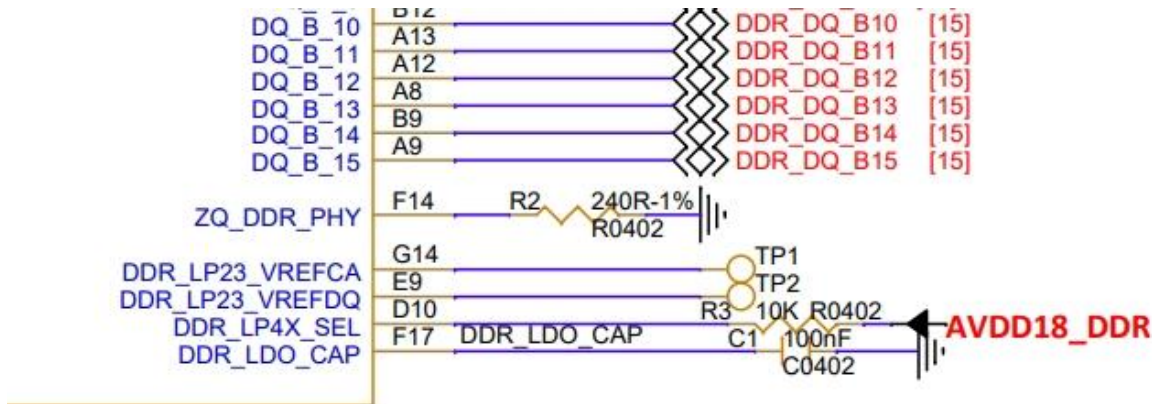


Key Stone® K1 Hardware Design Guide

1.1 External Circuit Requirements for the Minimal System

1.1.1 DDR Circuit Design

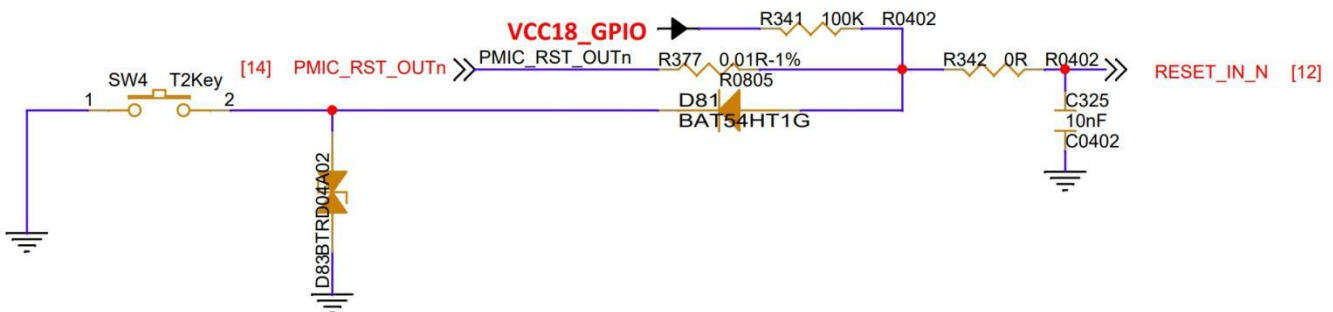
- Supports LPDDR4 / LPDDR4x.
- Pulling DDR_LP4x_SEL down to GND selects LPDDR4 mode; pulling it up to AVDD18_DDR selects LPDDR4x mode.
- The LPDDR4/4x external ZQ resistor must be $240\ \Omega \pm 1\%$, connected to GND.



Note:DDR routing must strictly follow the reference design provided by our company. Please refer to the hardware section in the release package for the official design files.

1.1.2 Reset

- Hardware reset of the chip is controlled externally and is active low.
- Add a 10 nF capacitor to the pin to suppress jitter and enhance noise immunity, preventing false resets.
- The pull-up supply for the RESET_IN_N net must match the IO power domain (i.e., pull up to VCC18_GPIO).
- The PGOOD signal from P1 connects directly to RESET_IN_N on K1, supporting push-button reset for both K1 + P1.
- If shared with other reset sources, add an OR gate or diode isolation.

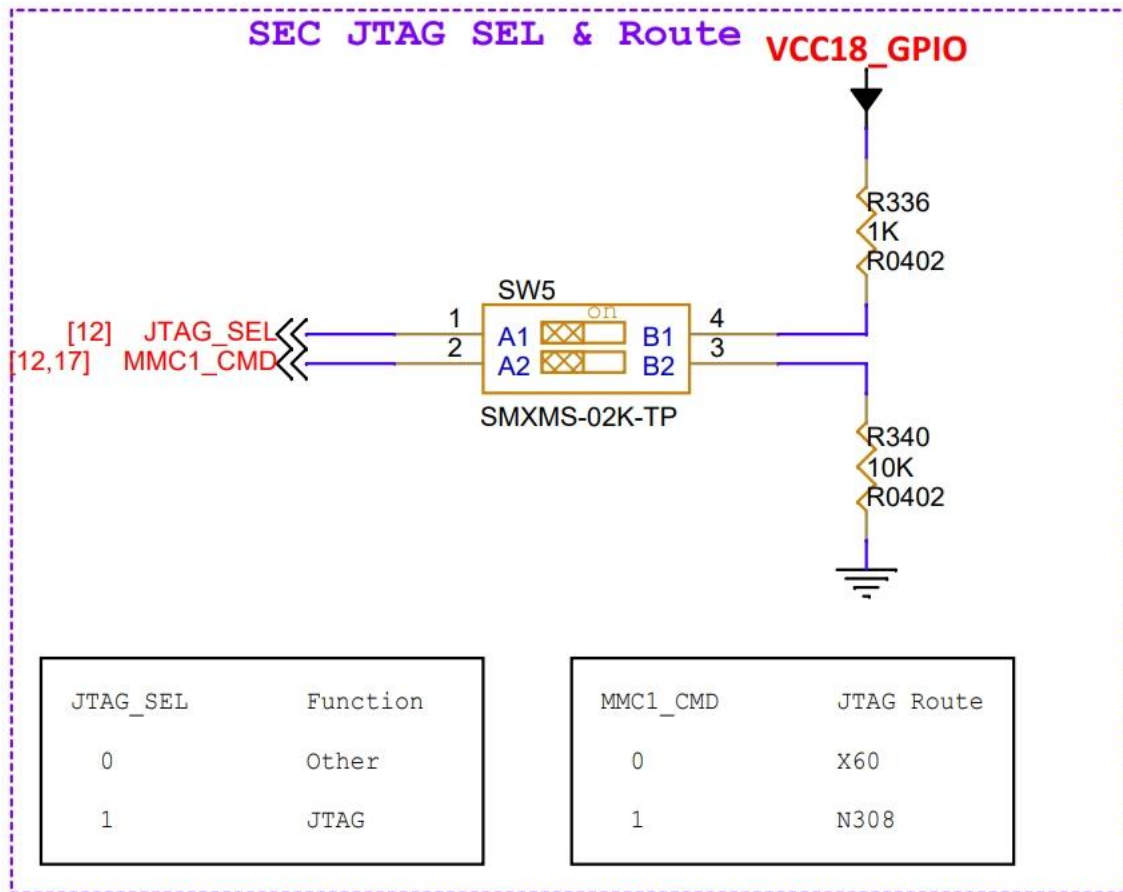


1.1.3 JTAG Interface

- Supports Primary JTAG and Sec2 JTAG.
- TDI, TMS, TCK, TDO, and Power/GND must connect to a J-Link debugger (signal voltage must match the Power domain).

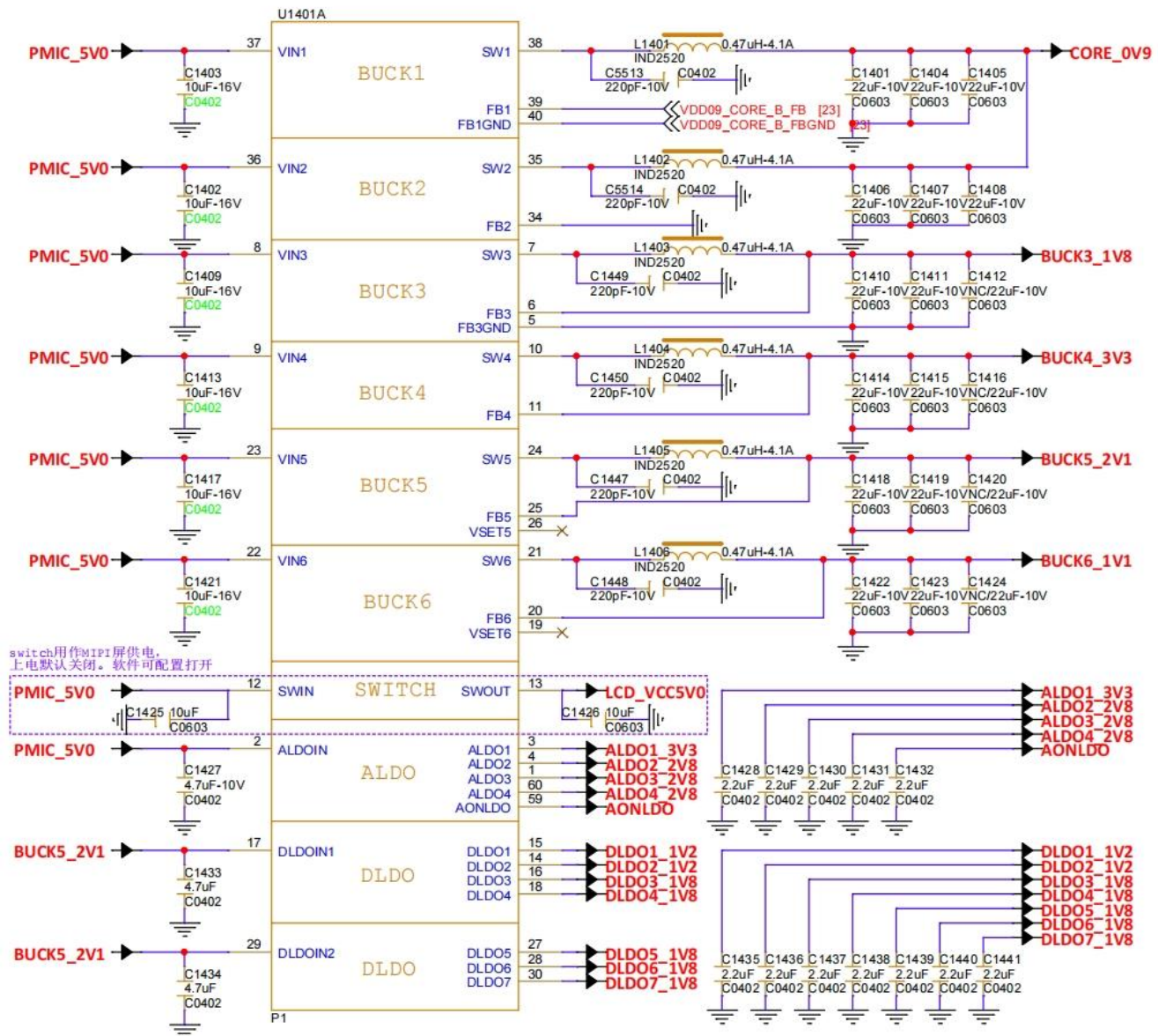
TRSTn should connect to the J-Link debugger or be pulled up to Power.

- When using Sec2 JTAG, pull up JTAG_SEL.
- Sec JTAG supports X60 / N308 CPU, controlled via MMC1_CMD.



1.1.4 Power Management (PMIC) Circuit Design

- P1 input supply is recommended to be 4V.
Vin3/Vin4 and Vin5/Vin6 must follow the reference PCB isolation guidelines.
- Add 220pF capacitors by default to SW1–SW6.
- The FB and FBGND pins of BUCK1/2 must connect directly to the main controller's FB/FBGND pins.
Keep routing away from noise-sensitive signals.



The P1 peripheral circuits must strictly follow our reference design. Please see the hardware files included in the release package.

1.1.5 Hardware Initialization and System Configuration Straps

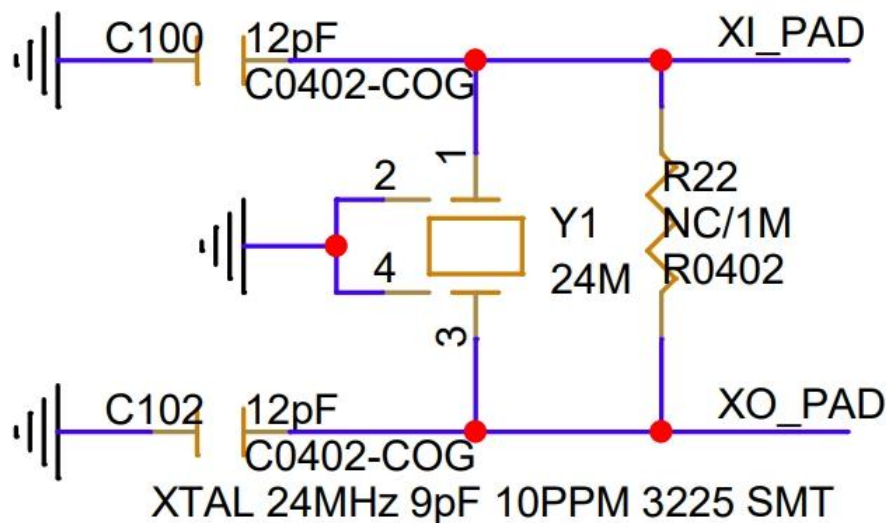
Signal Name	Direction	Description
QSPI_DATA3 / Strap3 FDL	I	Boot / Download selection 0: Boot 1: Download
QSPI_DATA2 / Strap2	I	Download interface selection 0: USB (USB0) 1: UART (UART0)

QSPI_DATA1 / Strap1 QSPI_DATA0 / Strap0	I	Boot device selection Strap1 & Strap0 00: eMMC 01: SPI NOR 10: SPI NAND 11: SD Card
GPIO_90 / Strap4	I	Flash voltage selection 0: 1.8V 1: 3.3V
JTAG_SEL	I	Sec JTAG selection 0: Other functions 1: SEC JTAG
MMC1_SD_CMD	I	JTAG Route 0: X60 1: N308

1.1.6 Clocking Circuit

The system clock is generated by the internal feedback circuitry in combination with an external 24 MHz crystal oscillator.

- Load capacitors must follow the crystal oscillator datasheet; 12 pF recommended.
- Reserve a 1 MΩ resistor in parallel between XIN and XOUT.



Note:

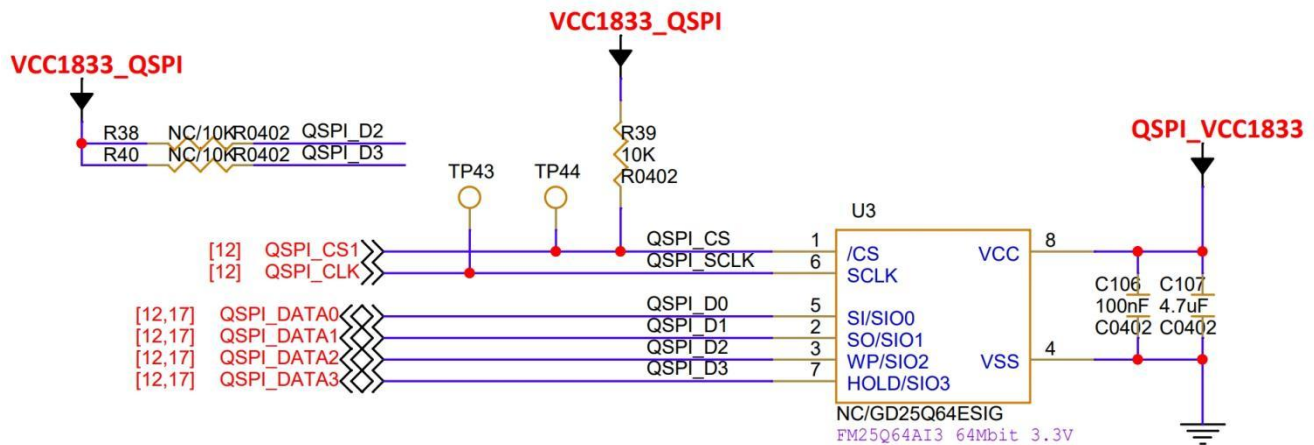
Ensure the chosen capacitors match the crystal's load requirement. Use NPO dielectric.

A 4-pin SMD crystal is recommended; connect the two GND pins solidly to the PCB ground to improve ESD robustness.

1.1.7 FLASH Schematic Design

- Quad-SPI serves as the interface for external serial flash with up to four bidirectional data lines.

- The Flash controller supports SPI NOR Flash and SPI NAND Flash.
- Supports 1.8V / 3.3V Flash; follow configuration based on VCC1833_QSPI power domain.
- Quad-SPI's four data pins are multiplexed with system configuration straps.
Fly-by routing is recommended. See Hardware Initialization Configuration.

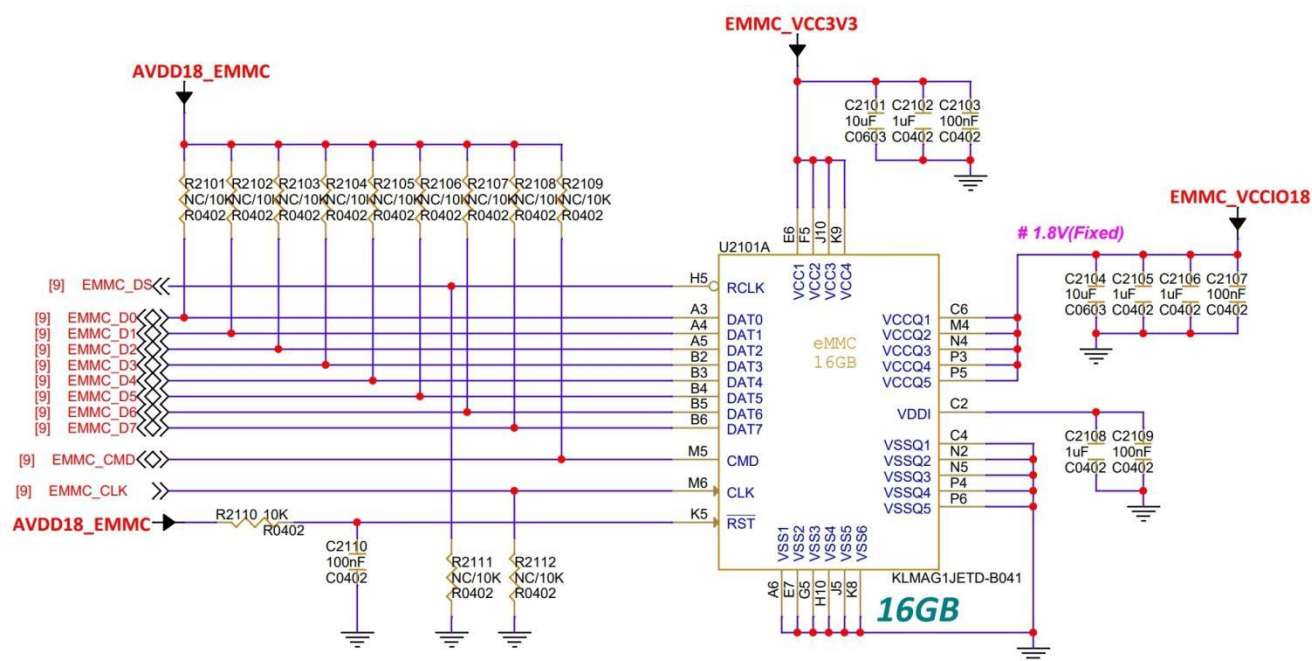


Note: No extra pull-ups are required for Flash data signals—internal configuration is already provided. Because the data pins are shared with boot straps, apply pull-up or pull-down resistors as required by your system configuration.

See Hardware Initialization Configuration above.

1.1.8 eMMC

- Compatible with 8-bit eMMC 5.1 specification.
- eMMC card supports SPI mode.
- External pull-ups/pull-downs for Data and DS are recommended as placeholders; mark as NC in mass production.
- Pay attention to length matching during layout.



1.2 Power Design Recommendations

1.2.1 CORE Power Design

The typical core voltage is 0.9 V to 1.05 V. Actual voltage is dynamically regulated by the remote-sense dynamic voltage adjustment circuit inside P1.

P1 BUCK1 and BUCK2 must be combined to supply the core rail.

The number and value of filtering capacitors have been verified through PI simulation. Follow the latest schematic exactly—do not modify these components.

Refer to the latest K1 schematic for details.

1.2.2 DDR Power Design

K1 supports LPDDR4 / LPDDR4x, with typical voltages 1.1 V / 0.6 V.

The DDR devices and the K1 DDR IO power must use the same power network.

As with the core rail, the number and value of filtering capacitors have been validated through PI simulation. Follow the latest schematic without changes.

See the latest K1 schematic.

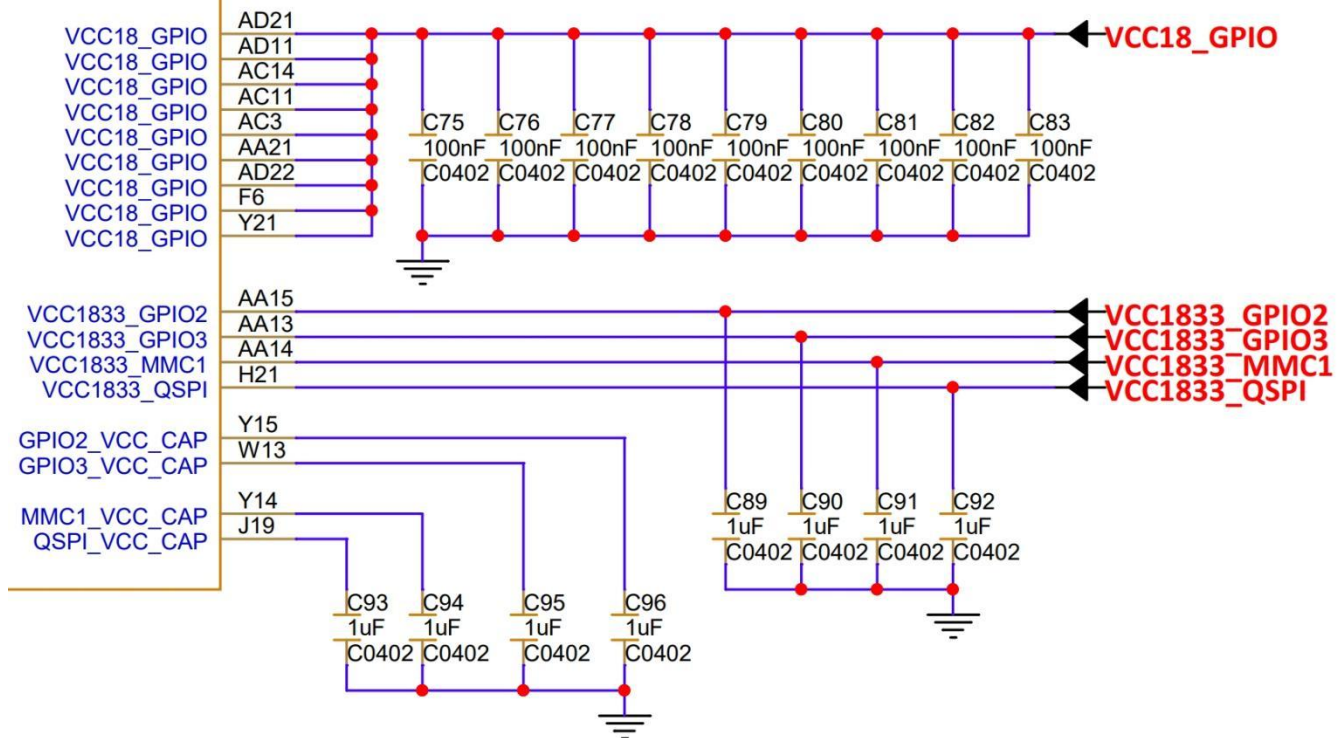
1.2.3 IO Power Design

- Pins named VCC18_GPIO must be supplied by a 1.8 V digital power rail.
- Pins named:
 - ✧ VCC1833_GPIO2 (GPIO75–80)
 - ✧ VCC1833_GPIO3 (GPIO47–52)
 - ✧ VCC1833_MMC1 (MMC1_DAT0–3, CMD, CLK)

✧ VCC1833_QSPI (QSPI_DAT0–3, CLK, CS1)

should be powered by 3.3 V or 1.8 V, depending on the peripheral device being used.

- A 0.1 μ F + 1 μ F capacitor pair must be placed near the VCC1833_GPIO2, VCC1833_GPIO3, VCC1833_MMC1, and VCC1833_QSPI pins, as shown below.



Note:

- GPIO90 configures the default QSPI operating voltage:
 - ✧ When GPIO90 is pulled up to 1.8 V, VCC1833_QSPI must operate at 3.3 V.
 - ✧ When GPIO90 is pulled down to GND, VCC1833_QSPI must operate at 1.8 V.
- Unused GPIO pins may remain floating, but each GPIO group's power rail must still be supplied.
- Modules such as HDMI, PCIEA/USB3.0, PCIEB, PCIEC, MIPI CSI, eMMC, USB2.0, MIPI DSI, etc., must also remain powered even if not used.

1.2.4 PLL Power Design

K1 includes two PLL power rails:

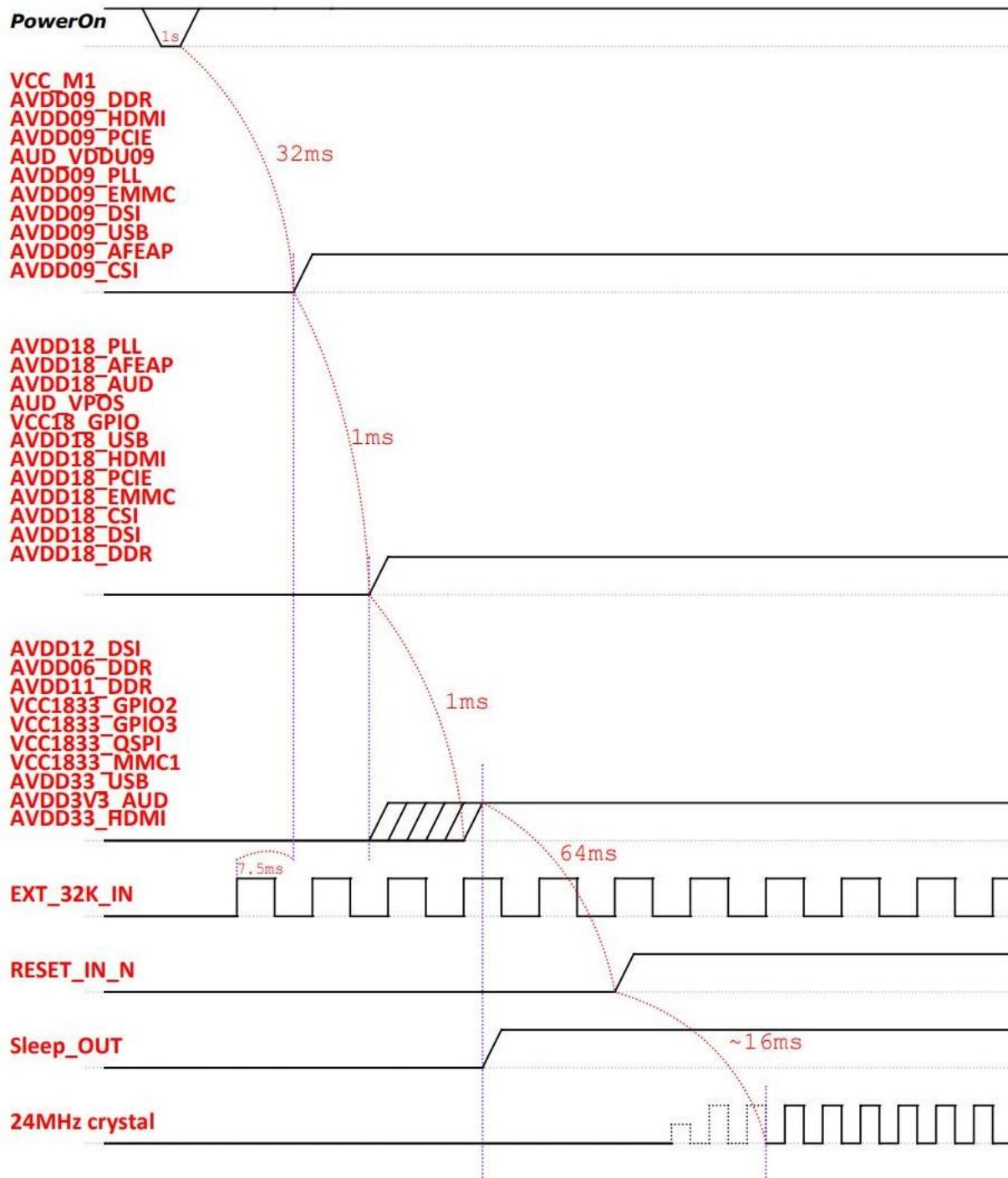
- AVDD09_PLL: Must be isolated using a ferrite bead (120 Ω @ 100 MHz, DC resistance $\leq$ 0.07 Ω). (This ferrite bead spec applies to all similar cases below.)
- AVDD18_PLL: Must also be isolated from the 1.8 V rail using a ferrite bead.

Refer to the latest P1 schematic.

1.2.5 Power-Up/Power-Down Sequencing

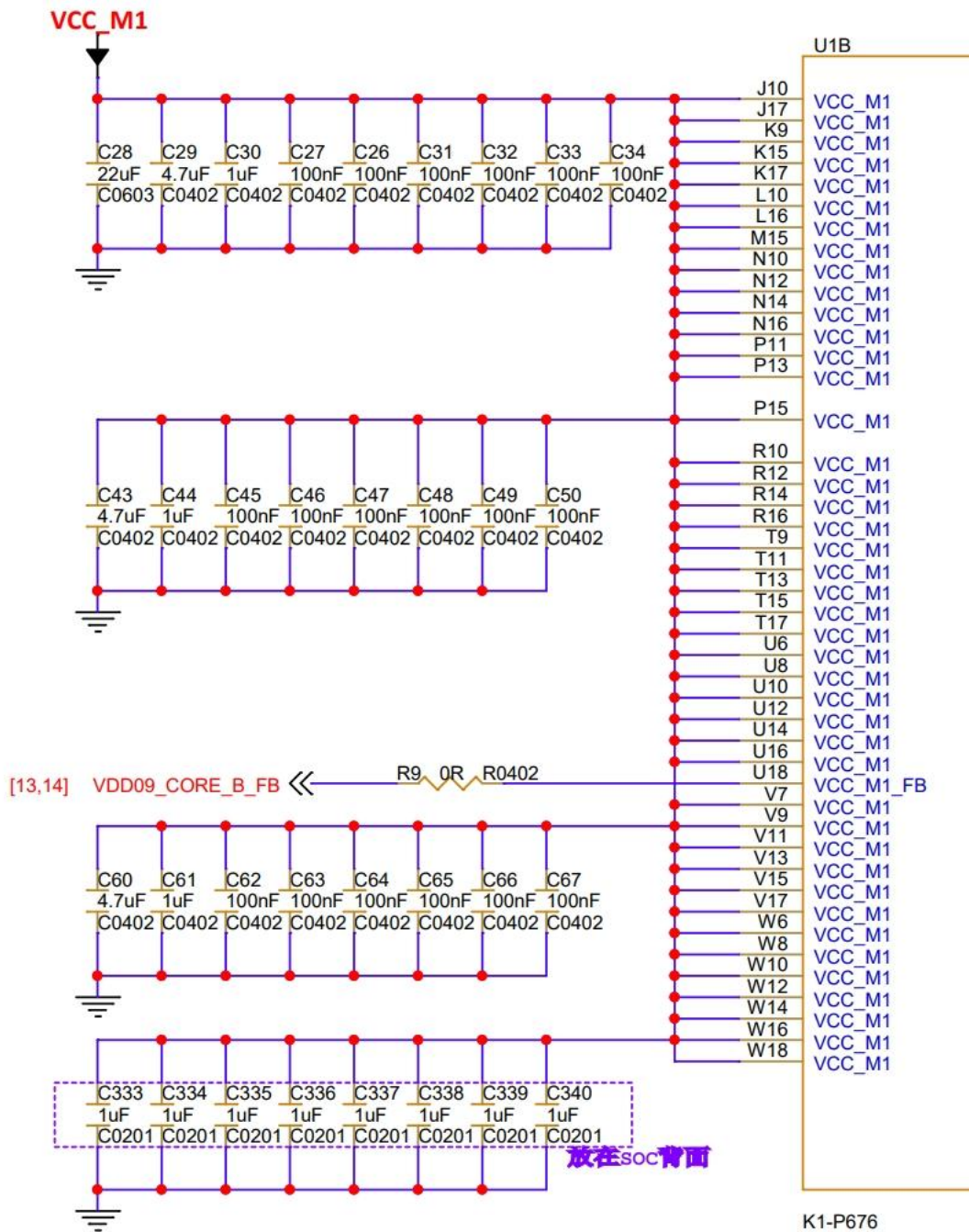
Core, DDR, and IO power rails follow specific sequencing requirements controlled by the PMIC P1.

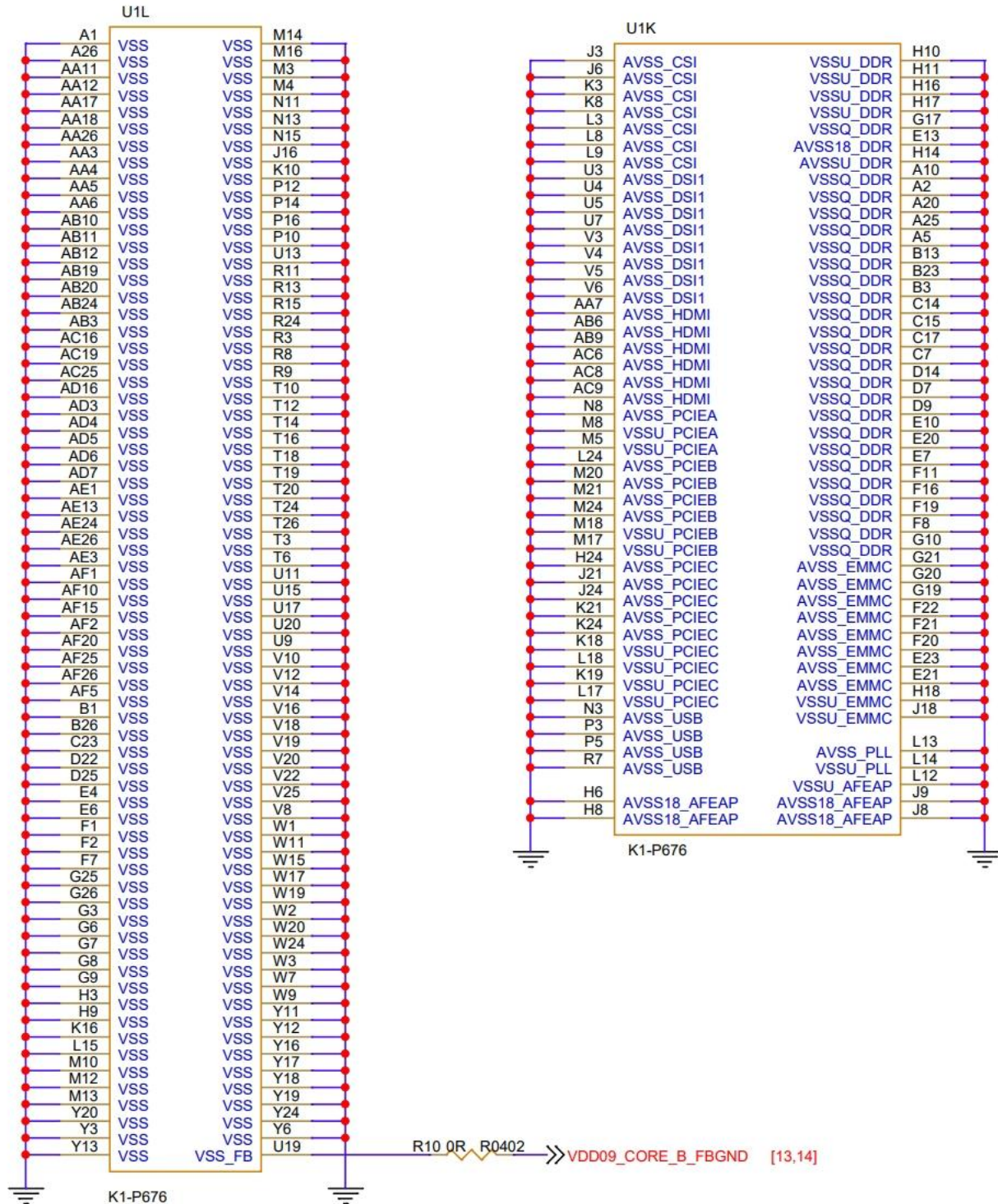
Refer to the latest schematic.



1.2.6 Remote-Sense Dynamic Voltage Scaling

- The K1 core power rail must support dynamic voltage scaling (DVS), enabling real-time adjustment of the DC-DC output.
- VDD09_CORE_B_FB must route from the main controller's VCC_M1_FB ball, and VDD09_CORE_B_FBGND must route from VSS_FB.





1.3 Analog Interface Design Guidelines

1.3.1 Analog Audio Interface Design

- The audio module's analog power rails (AUD_VDDU09, AVDD18_AUD, AVDD33_AUD) must be isolated from the system power rails using ferrite beads (recommended 120 Ω @ 100 MHz).

1.3.2 I2S Interfaces

- K1 supports four I2S interfaces.
 - ✧ I2S0 / I2S1 are controlled by the main CPU (X60).
 - ✧ R_I2S2 / R_I2S3 are controlled by the RCPU (N308).
- Each I2S interface can be configured as either master or slave.

1.3.3 MIPI CSI RX Interface Design

The differential video input supports 4-lane + 4-lane or 4-lane + 2-lane + 2-lane configurations.

In 4 + 2 + 2 mode, three cameras can stream simultaneously. However, the ISP can only process two streams; the third stream can only output YUV or RAW data directly through the CCIC DMA into DDR—it cannot be processed by the ISP.

- MIPI CSI1
 - ✧ Four differential data pairs sample against the MIPI_CSI0_CK1XP/N differential clock.
- MIPI CSI2
 - ✧ [2-lane mode]Differential pairs MIPI_CSI3_D2P/N and MIPI_CSI3_D3P/N sample against the MIPI_CSI2_CKP/N differential clock.
- MIPI CSI3
 - ✧ [2-lane mode]MIPI_CSI3_D0P/N and MIPI_CSI3_D1P/N sample against MIPI_CSI3_CKP/N.
 - ✧ [4-lane mode]Four pairs (D0P/N, D1P/N, D2P/N, D3P/N) sample against MIPI_CSI3_CKP/N.

Power requirements:

- AVDD09_CSI must be isolated from the digital power rail using a ferrite bead; place two 1 μ F capacitors near the chip pins.
- AVDD18_CSI must also be isolated with a ferrite bead; place one 1 μ F capacitor near the chip pins.

1.3.4 MIPI DSI TX Interface Design

- K1 integrates one MIPI TX PHY for connecting to MIPI-based LCD panels.
- AVDD18_DSI must be isolated from the digital power rail using a ferrite bead.

Refer to the latest K1 schematic for detailed design.

1.3.5 SPI LCD Interface Design

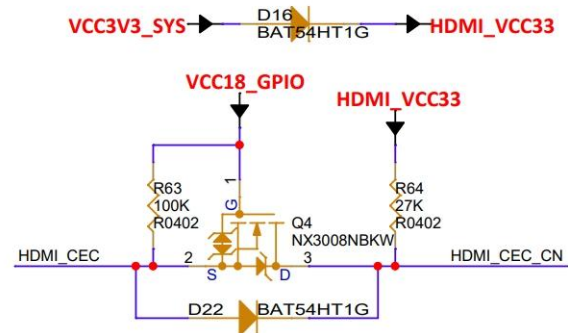
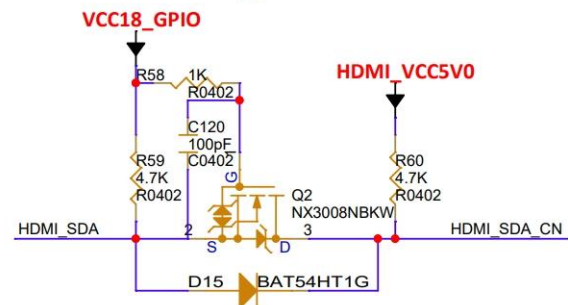
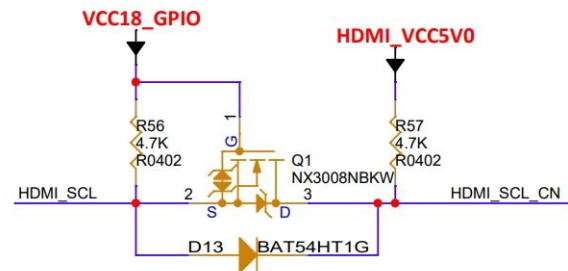
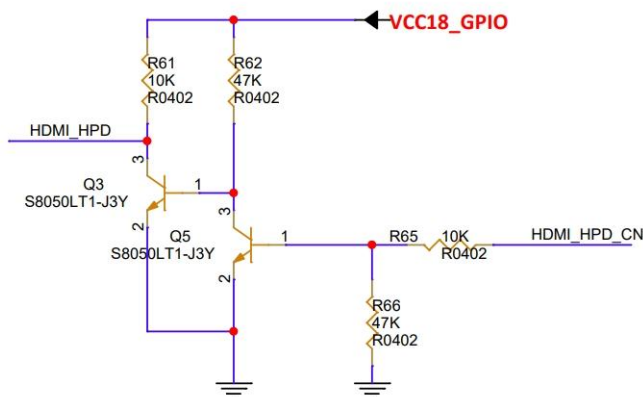
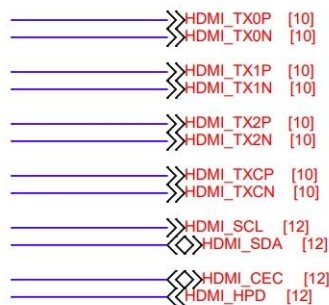
- Supports 1-wire serial peripheral SPI display data transfer.
- Data pin is SPILCD_DOUT0 or SPILCD_DIN.

Note:The LCD_TE signal cannot be used simultaneously for both SPI LCD and MIPI DSI LCD.

1.3.6 HDMI Interface Design

- K1 includes an integrated HDMI PHY.
- HDMI power rails (AVDD33_HDMI, AVDD18_HDMI) must be isolated from the digital power rails using ferrite beads.
 - ✧ Place two 1 μ F capacitors near the chip pins.
 - ✧ AVDD33_HDMI must be supplied through a MOSFET switch circuit, with two 1 μ F capacitors near the pins.
- HDMI signals require ESD protection. ESD components must be placed close to the HDMI connector with parasitic capacitance < 0.3 pF.
- HDMI_SCL, HDMI_SDA, HDMI_CEC, HDMI_HPD require external circuitry:
 - ✧ HDMI_SCL / HDMI_SDA must be level-shifted to 5 V
 - ✧ HDMI_CEC must be level-shifted to 3.3 V
 - ✧ Incoming HDMI_HPD must be level-shifted to 1.8 V before entering the SoC
 (See the figure below for the specific design.)

HDMI



For complete schematic details, refer to the official K1 schematic design files.

- Power rails AVDD18_PCIEA, AVDD18_PCIEB, AVDD18_PCIEC should be combined and isolated from digital power using ferrite beads; place three 1 μ F capacitors near each pin.

Note: Regardless of which PCIe is used, PCIEA_R_EXT must always be pulled up to AVDD09_PCIE via a 240 Ω 1% resistor.

- PCIE_RXP/N
 - ✧ If connecting to an IC, each RX differential pair must include a 220 nF series capacitor at the IC side.
 - ✧ If connecting to a PCIe slot, the RX differential pairs connect directly without series capacitors.
- PCIE_TXP/N
 - ✧ Each TX differential pair must include a 220 nF series capacitor at the K1 side for AC coupling.
- PCIE_REFCLKP/N supports two clock schemes:
 - ✧ K1 provides the clock to the device. Differential signals connect directly.
 - ✧ External device provides the clock to K1. Differential signals at the device source must include a 49.9 Ω pull-down resistor. Clock deviation tolerance: ± 300 ppm, compliant with PCIe specification.

1.4.3 UART

K1 provides 12 UART interfaces, divided into X60 UART and N308 UART:

- X60 UART: 10 interfaces
 - ✧ UART0: 2-wire debug port
 - ✧ UART1–UART9: 4-wire ports
 - ✧ UART3 can be used for the secure domain
- N308 UART: 2 interfaces, currently unsupported; consult FAE if needed.

1.4.4 I2C

K1 provides 10 I2C interfaces, categorized into AP I2C, HDMI I2C, PWR I2C:

- AP I2C: 8 interfaces (I2C0–I2C7) for peripheral control; I2C0, I2C1, I2C7 are used for camera control.
- HDMI I2C: 1 interface (HDMI_I2C) for HDMI interface control.
- PWR I2C: 1 interface (PWR) for power IC configuration.

1.4.5 MMC

- K1 has two MMC interfaces:
 - ✧ MMC1 supports 3.3 V / 1.8 V logic levels
 - ✧ MMC2 supports 1.8 V only
- MMC1/2 can interface with SDIO Wi-Fi or SD Cards.

1.4.6 USB 3.0

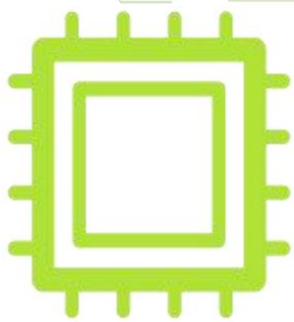
- K1 supports one USB 3.0 port, shared with PCIEA.
- ESD protection is required; device parasitic capacitance should be < 0.5 pF and placed close to the USB connector.
- Signal handling:
 - ✧ USB3_RXP/N
 - If connecting to an IC or module, series 100 nF capacitors are required at the IC/module side.

- If connecting to a socket, the differential pairs connect directly to the socket without series capacitors.
- ✧ USB3_TXP/N
 - If connecting to an IC or module, series 100 nF capacitors are required at the K1 side.
 - If connecting to a socket, series 100 nF capacitors should be placed near the socket.

Note: Regardless of using USB 3.0 or any PCIe, PCIEA_R_EXT must always be pulled up to AVDD09_PCIE via a 240 Ω 1% resistor.

Chapter 2

PCB Design



Key Stone® K1 Hardware Design Guide

2.1 PCB Stack-up Design

To minimize signal reflection during high-speed transmission, impedance matching must be maintained at the source, receiver, and along the transmission lines. The impedance of a single-ended trace depends on its trace width and distance to the reference plane. For differential pairs, trace width and spacing depend on the selected PCB stack-up.

Since minimum trace width and spacing are constrained by PCB type and cost, the chosen stack-up must satisfy all impedance requirements, including inner/outer layers, single-ended, and differential lines.

Stack-up design principles:

1. Layers adjacent to components should be ground planes to provide reference for routing.
2. All signal layers should be as close to ground planes as possible.
3. Avoid placing two signal layers adjacent to each other.
4. High-current power layers should be adjacent to ground planes if possible.
5. Stack-up should be symmetrical.

K1 currently uses a 6-layer stack-up. The reference stack-up is shown below. If using another stack-up, recalculate impedance according to the PCB manufacturer's specifications.

6-layer reference stack-up:

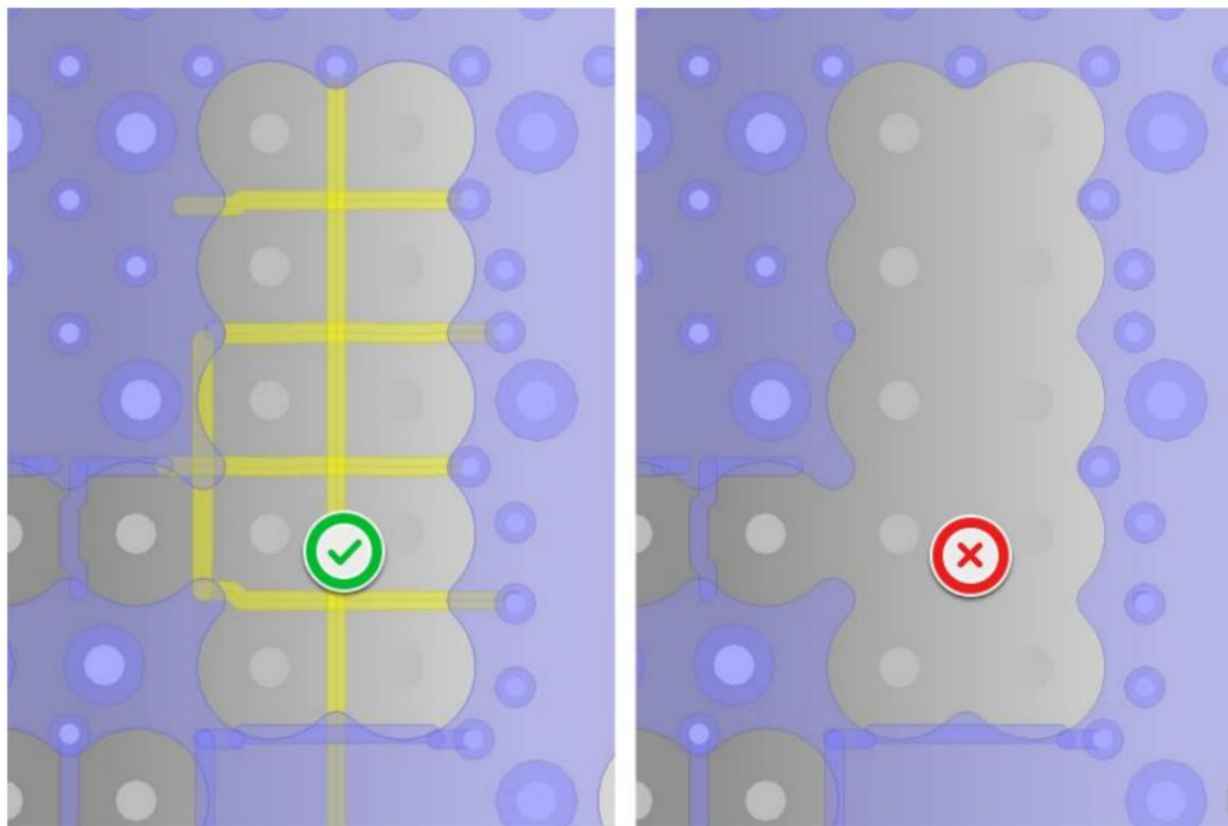
- Signal layers: L1 / L3 / L4 / L6
- Reference planes: L2 / L5 (complete planes)

Customer Stack-up			CEE Stack-up Information				Impedance					
Layer		Copper Weight (oz)	Thickness	Proposed Thickness	Vendor	Family	Structure	Reference Layer	Single End		Differential	
									50+/-5ohm		90+/-9ohm	
									Customer Design LW	Adjusted LW	Customer Design LW/LS	Adjusted LW/LS
Top Soldermask												
L1	cct01	0.42OZ+Plating		1.636				L2	5	4.86	4/4.7 4/5.2	4/4.7 4.225/4.97 5
	Prepreg		3.048	3.048	生益	S1000-2MB	1080*1					
L2	sgt02	1OZ		1.2								
	Core		6.337	3.937	生益	S1000-2M						
L3	sgb03	1OZ		1.2				L4/L2	5	5	4/5.2	4/5.2
	Prepreg		4.512	4.512	生益	S1000-2MB	2116*1					
	Full Etched Core		30.118	30.118	生益	S1000-2M						
	Prepreg		4.397	4.397	生益	S1000-2MB	2116*1					
L4	sgt04	1OZ		1.2				L3/L5	5	5	4/5.2	4/5.2
	Core		6.337	3.937	生益	S1000-2M						
L5	sgb05	1OZ		1.2								
	Prepreg		3.048	3.048	生益	S1000-2MB	1080*1					
L6	cct06	0.42OZ+Plating		1.636				L5	5	4.86	4/4.7 4/5.2	4/4.7 4.225/4.97 5
Bottom Soldermask												
Overall Thickness				61.069								

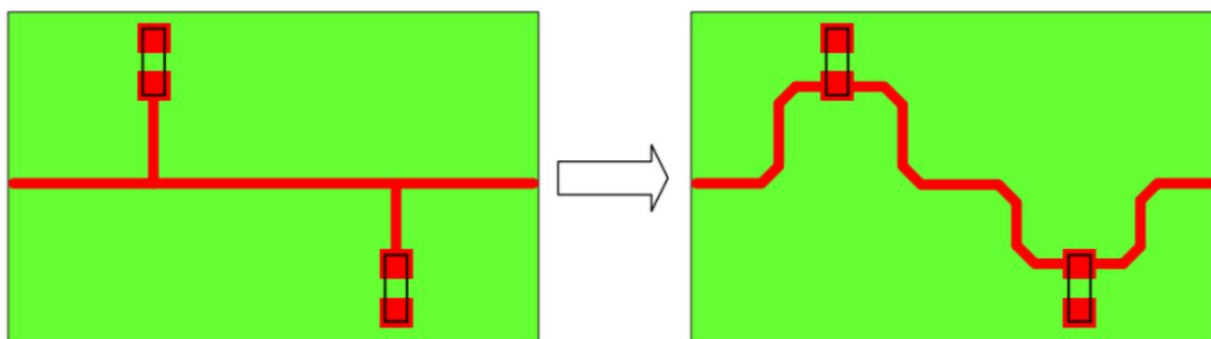
2.2 General Routing Guidelines

1. Avoid right angles or sharp corners in traces.
2. Keep traces away from clock components (crystals, oscillators, clock generators/distributors), switching power supplies, and magnetic components.
3. Ensure traces have continuous reference planes.

4. In BGA areas, connect separated planes using traces as shown:

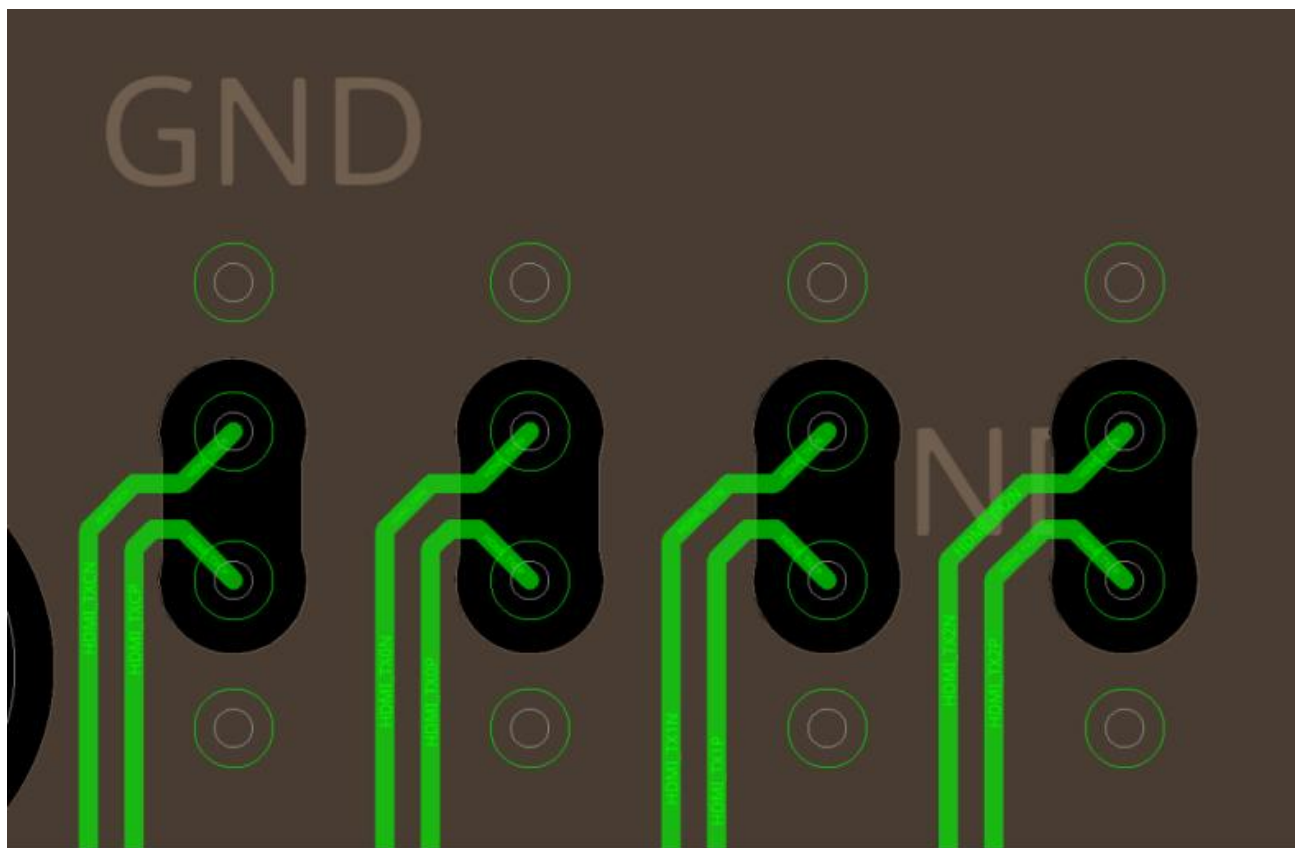


5. Minimize stub lengths; recommended stub length is 0:

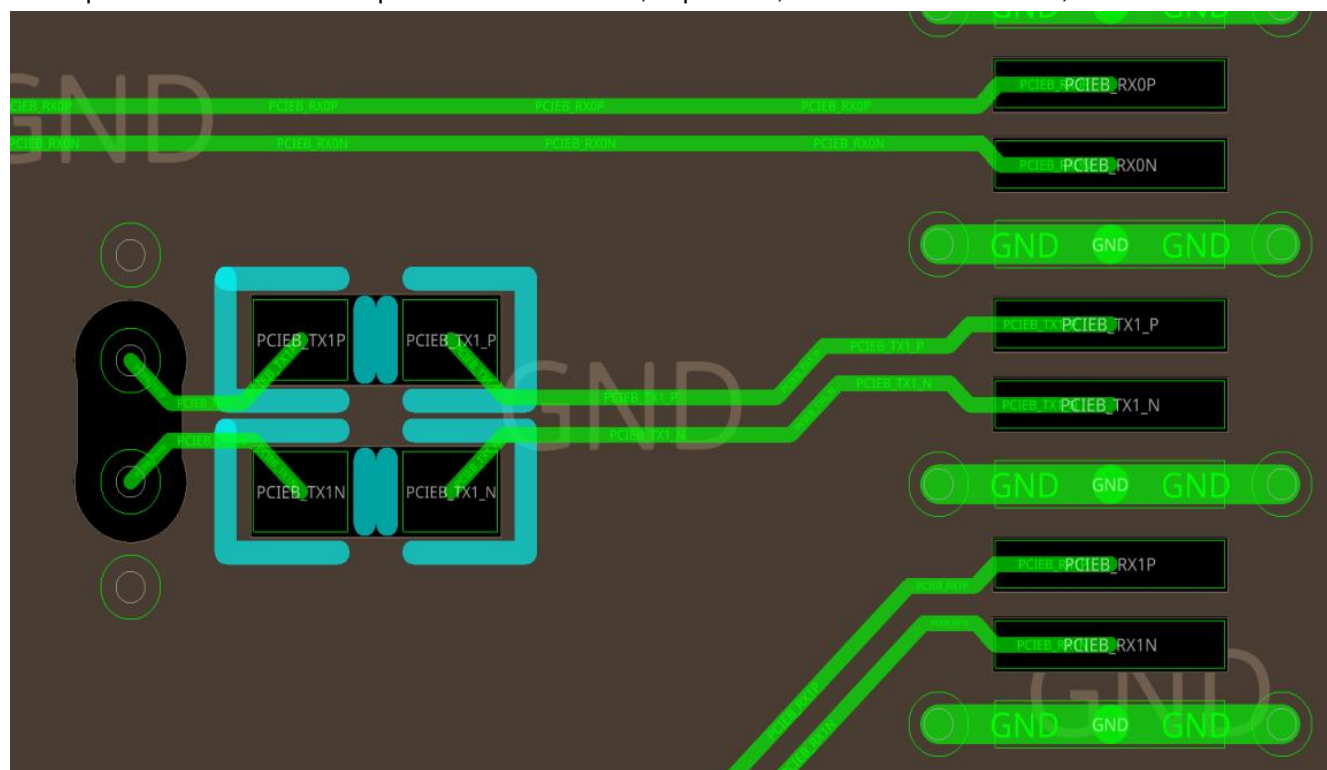


High-speed signal routing recommendations:

1. When changing layers, add GND vias next to signal vias to maintain a continuous return path:



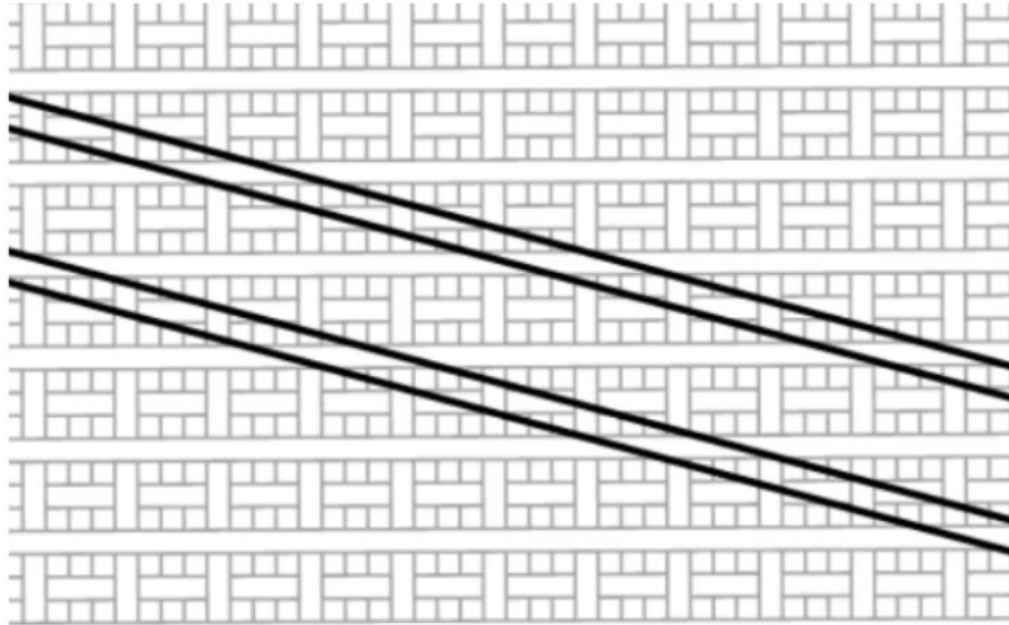
2. Surface-mount pads reduce impedance; to mitigate discontinuities, remove the reference plane under the pad. Common SMD components: ESD devices, capacitors, common-mode chokes, connectors.



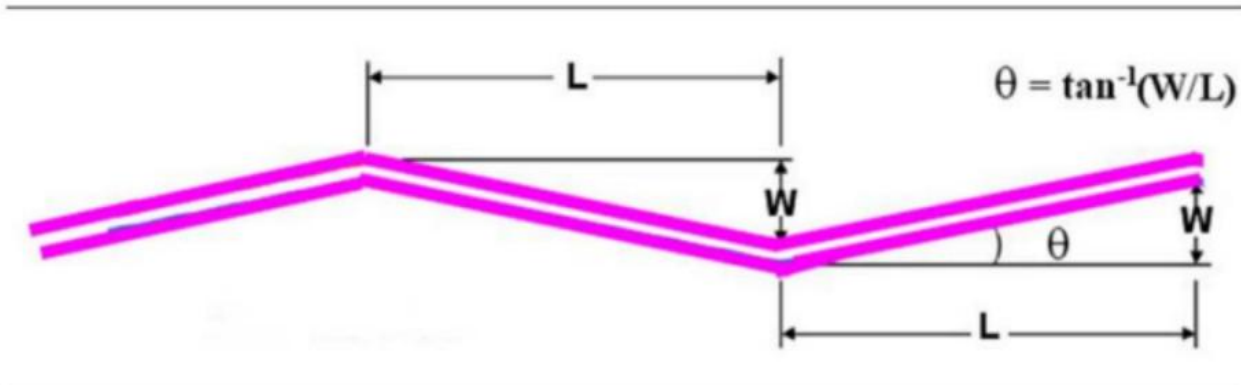
3. Avoid glass fiber weaving effects:

- The dielectric constant varies locally due to glass fiber weave gaps, causing impedance fluctuations and skew in differential pairs.
- For interfaces ≥ 8 GT/s and trace length > 1.5 in, glass fiber effects must be mitigated:

Method 1: Route traces at 10° angles or rotate PCB material 10° during fabrication.



Method 2: Use Zig-Zag routing; width $W \geq 3 \times$ glass fiber spacing. Recommended: $W=60\text{mil}$, $\theta=10^\circ$, $L=340\text{mil}$.

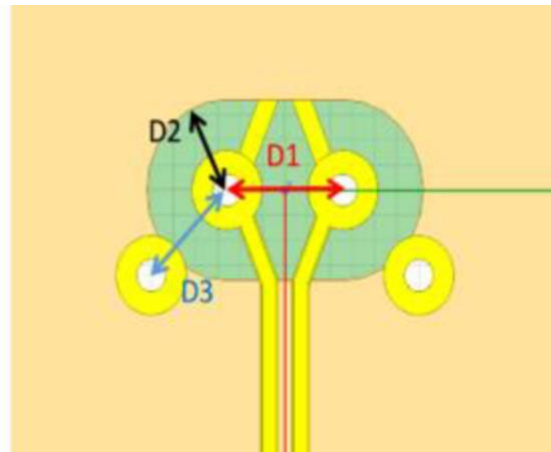
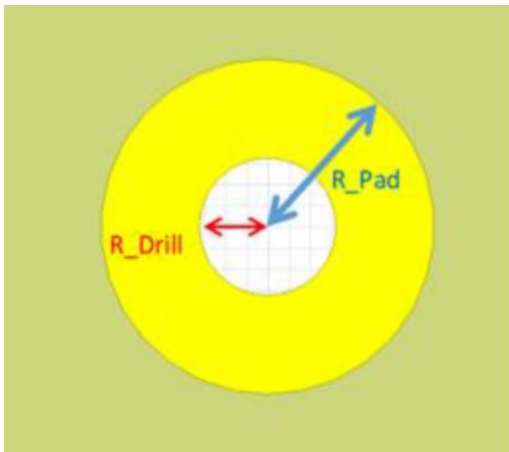


4. Minimize layer changes; if necessary, consider Via Stubs and keep them short.

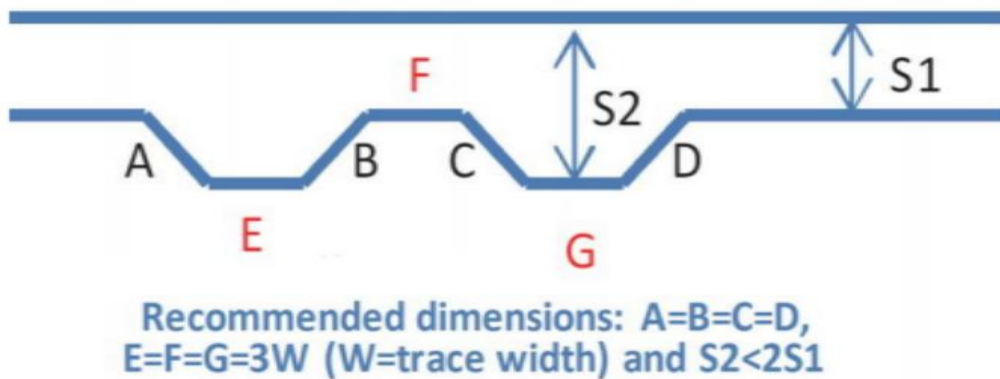
5. Differential via recommendations (for 8 GT/s interfaces):

Add Dog-Bone structures; optimize dimensions via simulation. Reference for EVB 1st-order HDI:

- ✧ R Drill = 4 mil (Drill radius)
- ✧ R Pad = 16 mil (Pad radius)
- ✧ D1 = 30 mil (differential via center spacing)
- ✧ D2 = 15 mil (back-side pad size)
- ✧ D3 = 30 mil (signal via to return via center spacing)

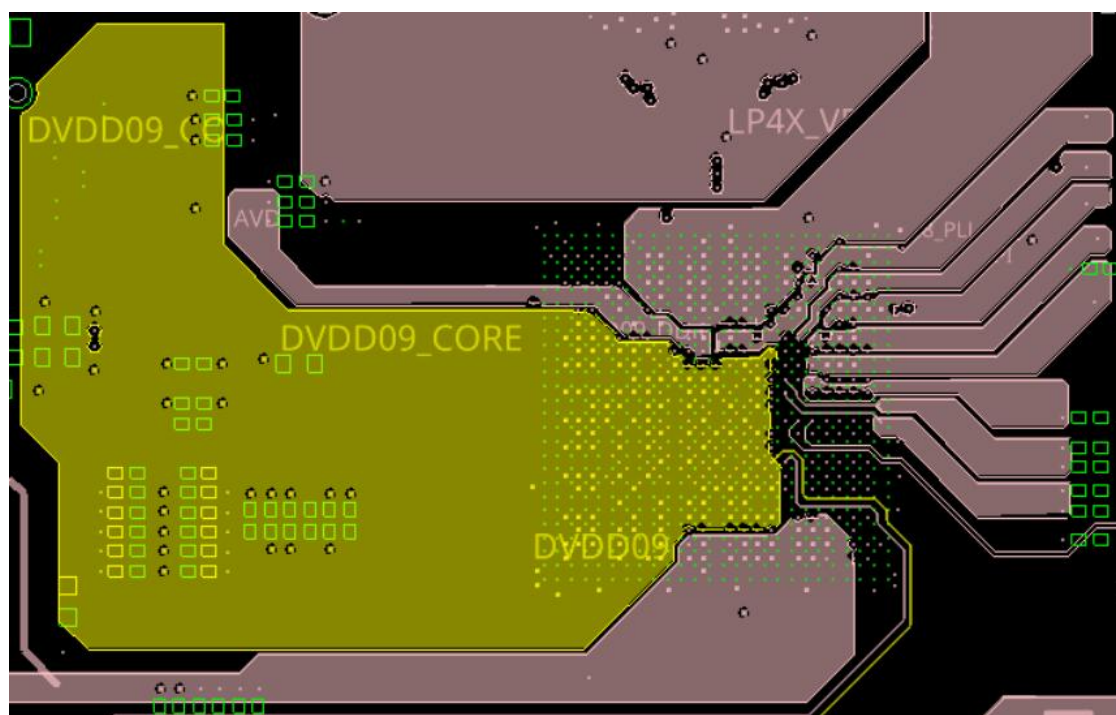
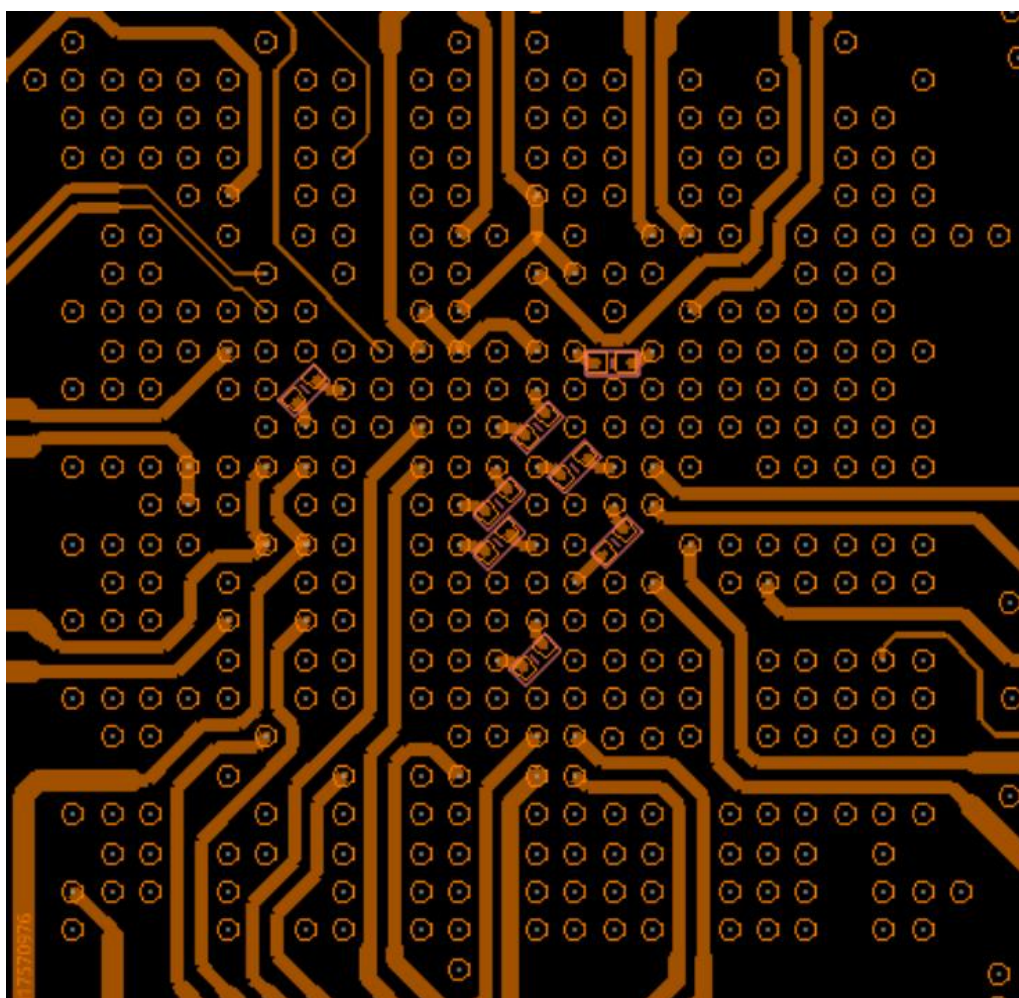


6. Differential pairs: length mismatch ≤ 5 mil. When routing compensation is needed, ensure trace shapes minimize impedance discontinuities:



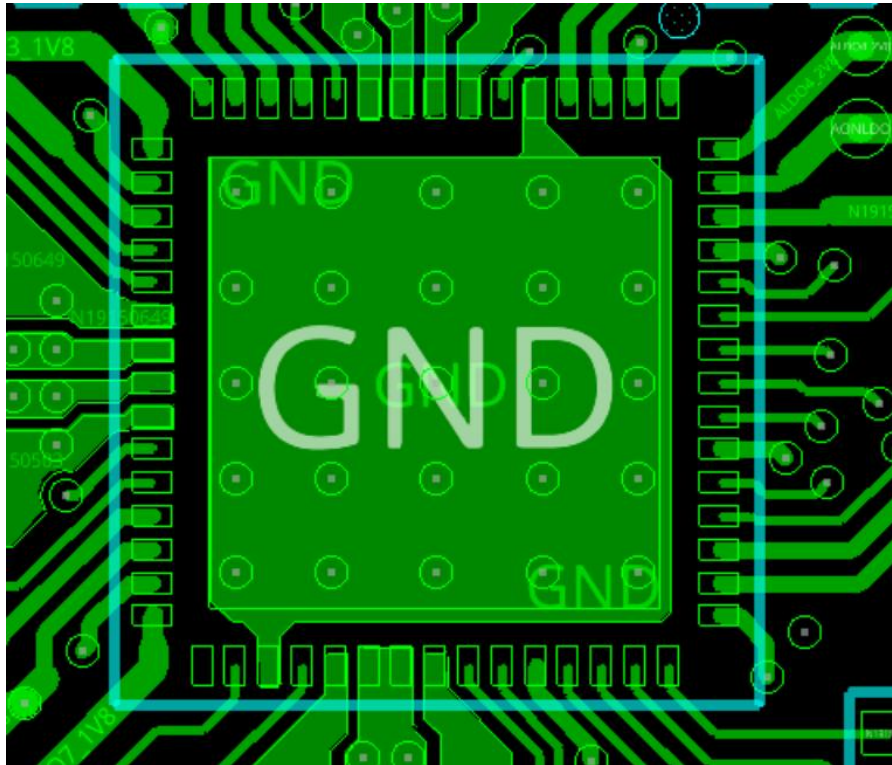
2.3 Power and Decoupling Capacitor Design

1. Place decoupling capacitors close to the pins; use short, thick traces to vias for power and GND.
2. Power planes should be short and wide; avoid fragmentation by too many vias.
3. For proper PI analysis, use our reference capacitor selection; do not reduce capacitor count.
4. Via placement should follow our reference design, do not remove power or ground vias.

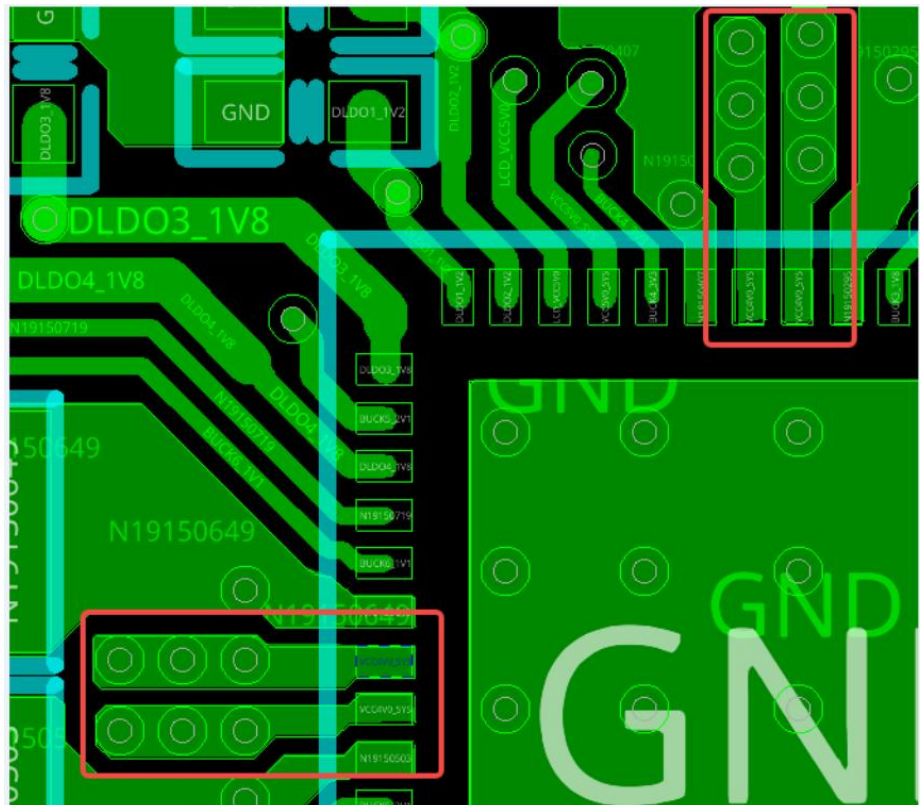


2.4 P1 Power Layout Design

1. Place ground via arrays evenly under central thermal pads:

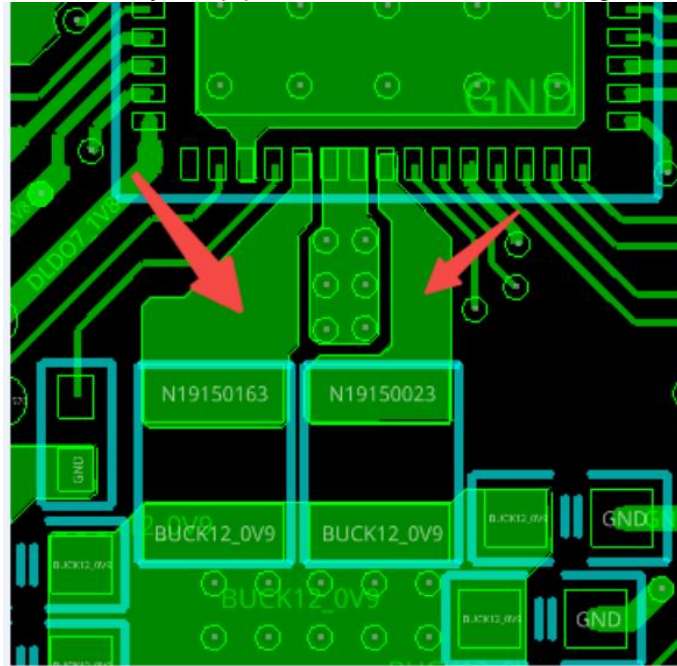


2. BUCK3–6 Vin traces should be separate; BUCK1/2 can share copper. Use three vias per pin:



-

5. Handle SW copper pours carefully, keep paths short, and route other signals away from SW traces:

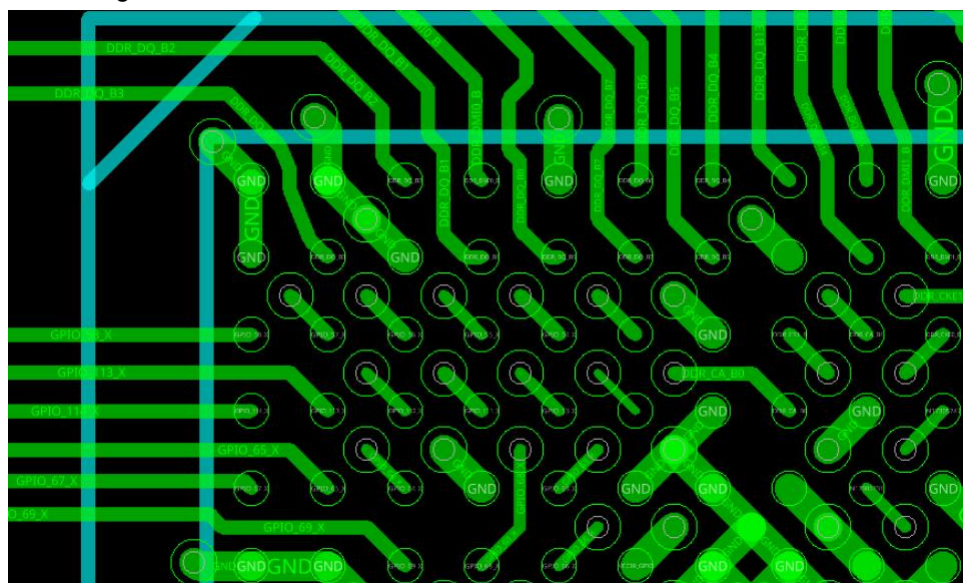


2.5 Subsystem Design

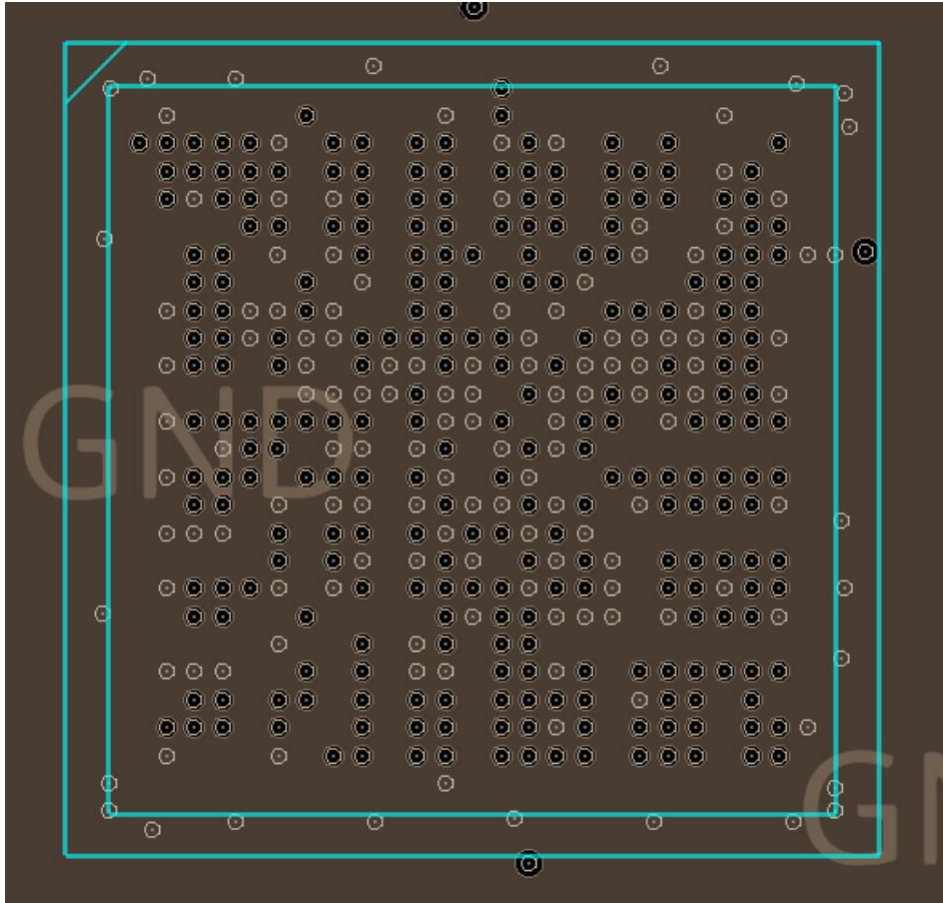
For a small system composed of CPU – DDR – eMMC, we strongly recommend using our reference board design, which has been fully simulated and verified. Designing your own board requires strict simulation and verification, and carries high risk.

2.5.1 CPU – PCB Layout Recommended Design

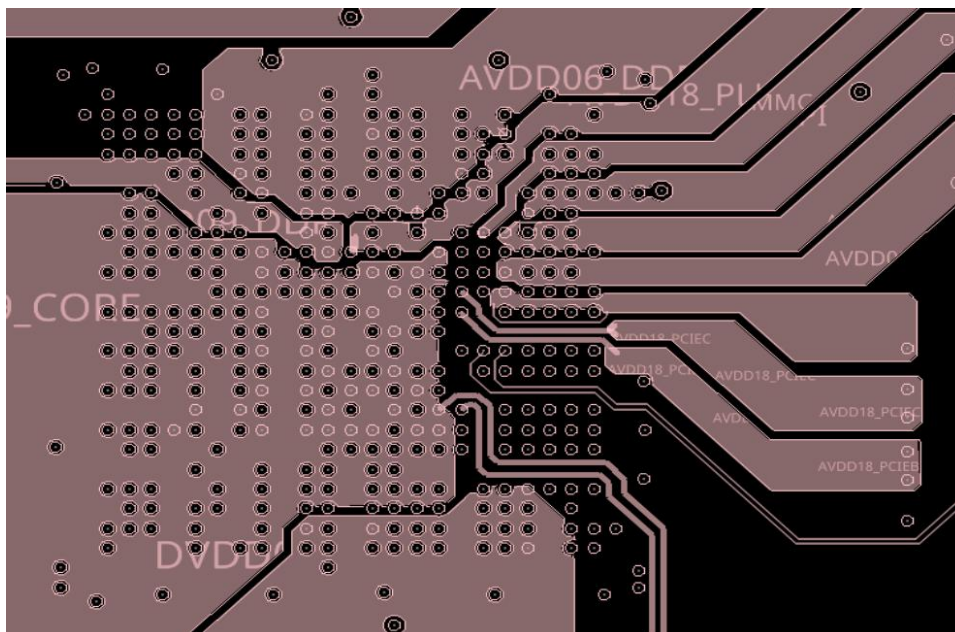
1. Outer CPU balls can fan out on the top layer using 5mil traces. The second row can route between the first-row balls using 5mil traces:



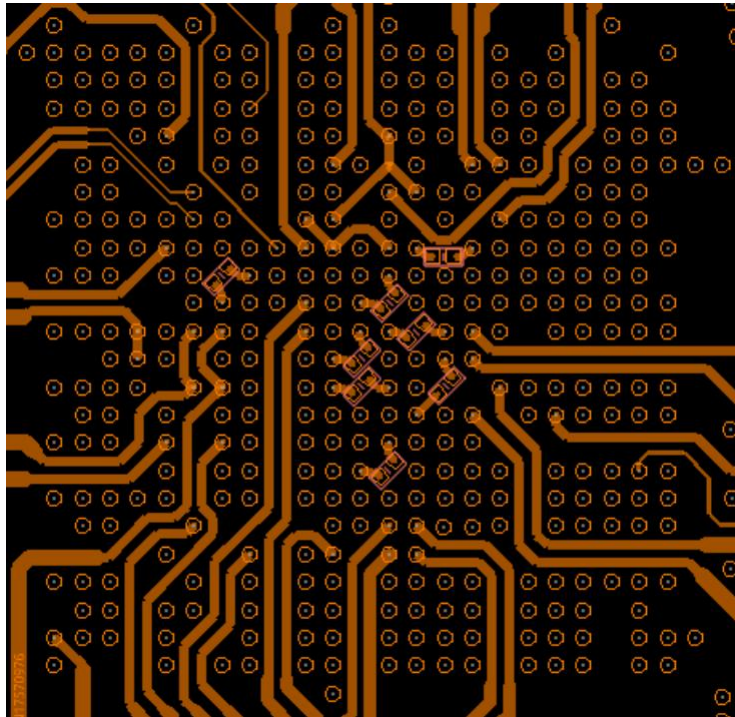
2. Inner CPU balls: if signals occupy the first and second rows, starting from the third row, route to inner layers. Place vias regularly to leave wide channels for ground and power planes. Copper fills on ground layers with multiple channels connected to the outer ground improve SI/PI and thermal performance:



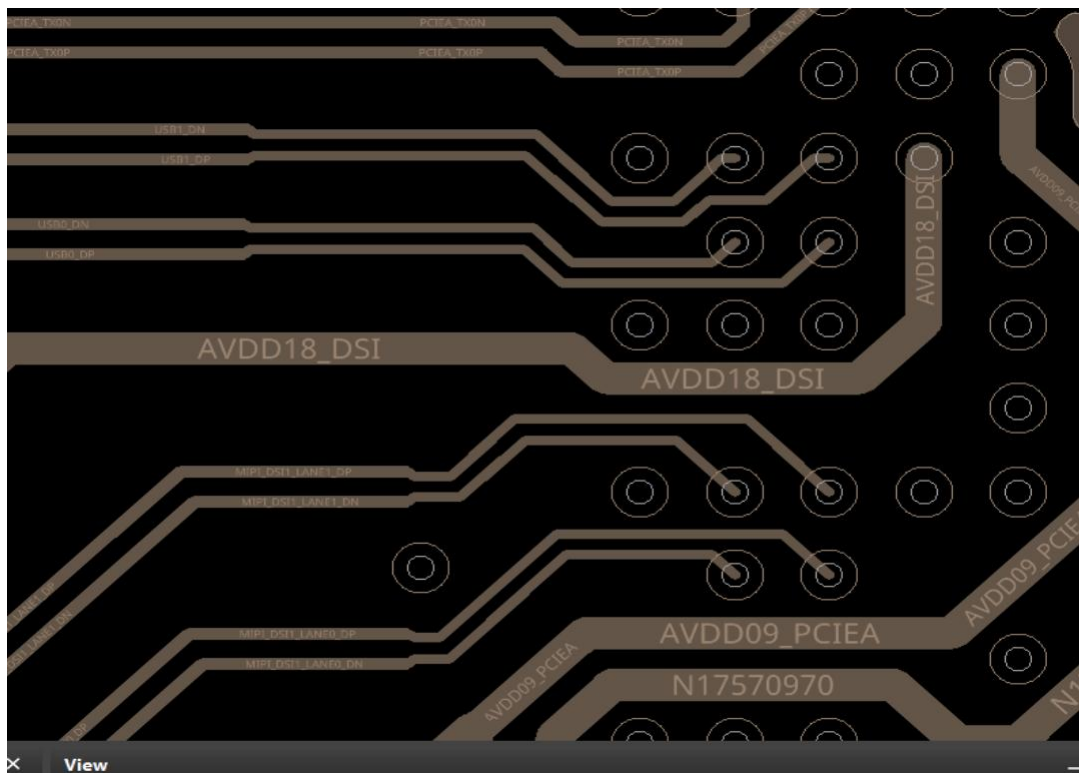
3. Power plane copper fills: place vias systematically to maximize copper for each power net, improving power integrity:



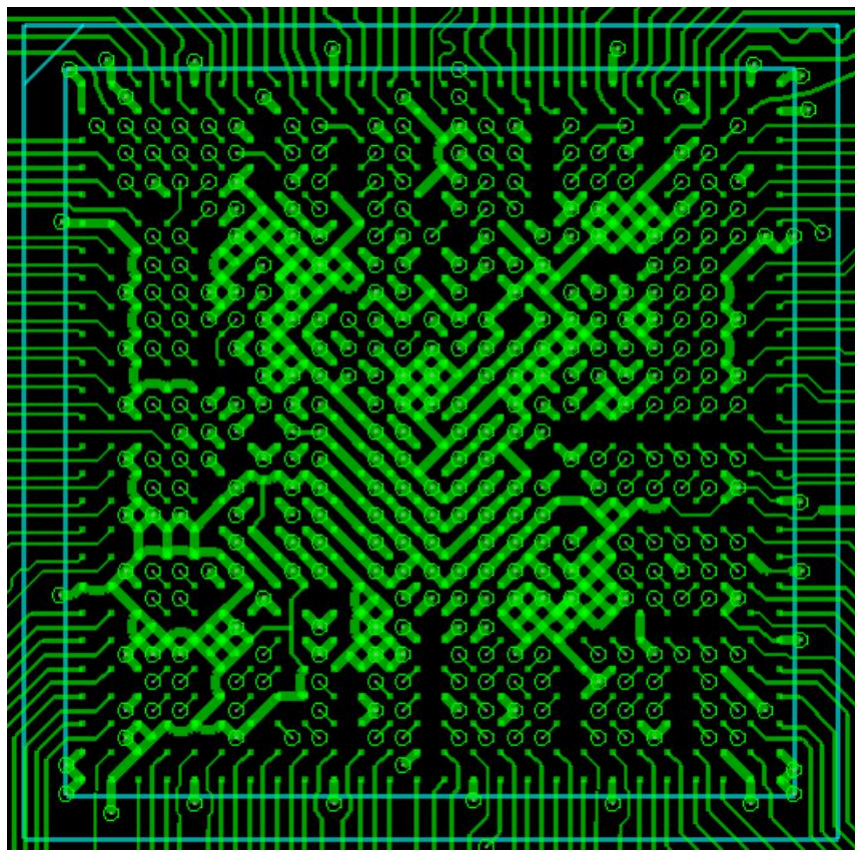
4. Capacitor placement on the CPU backside: place capacitors at relevant pins; add as many as possible where space allows to improve PI:



5. If trace routing is difficult near the CPU, temporarily reduce trace width using a neck, but restore to normal width after leaving the CPU area:



6. Top-layer power and ground: connect with short, thick traces as shown:



7. Core power feedback line: route from the farthest end of the power plane with minimal layer changes.

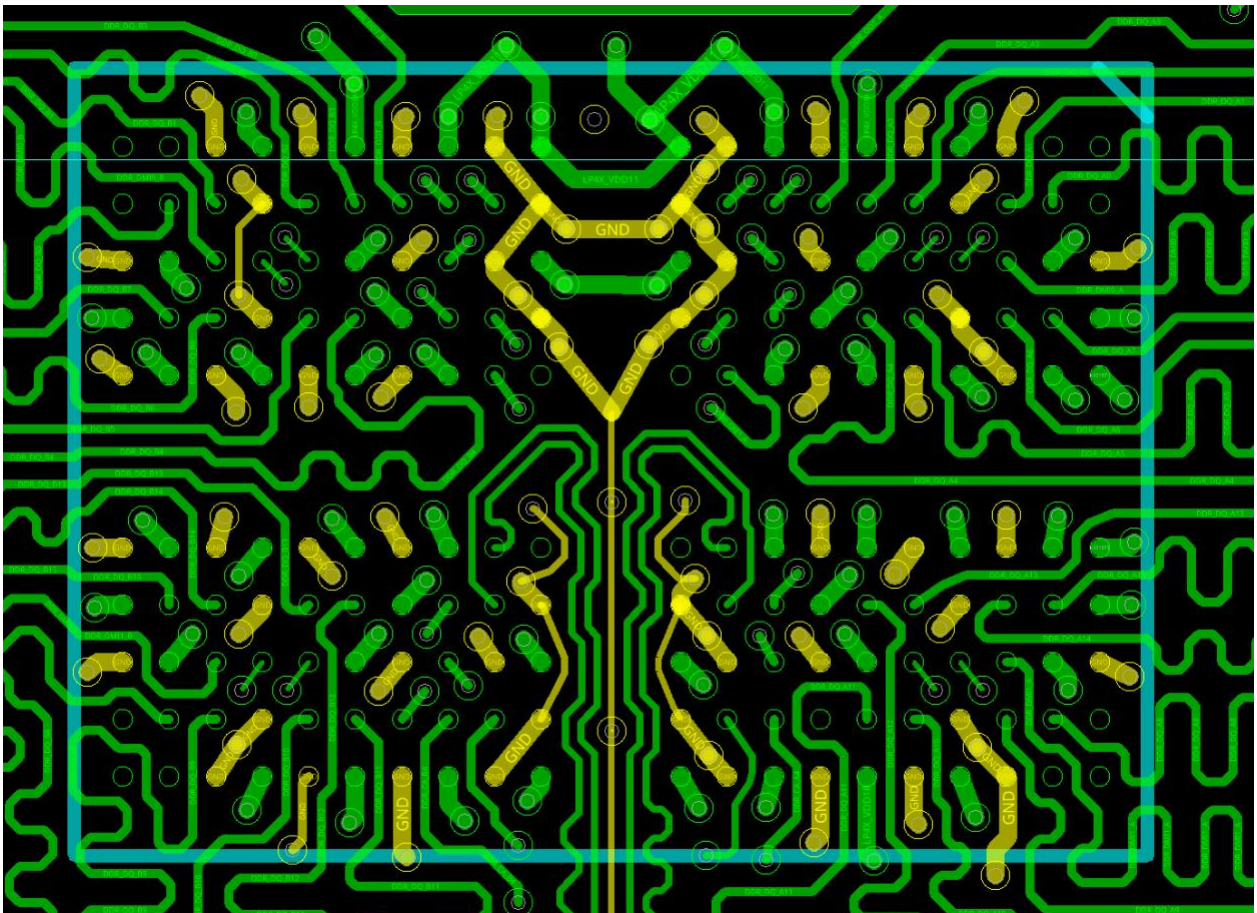
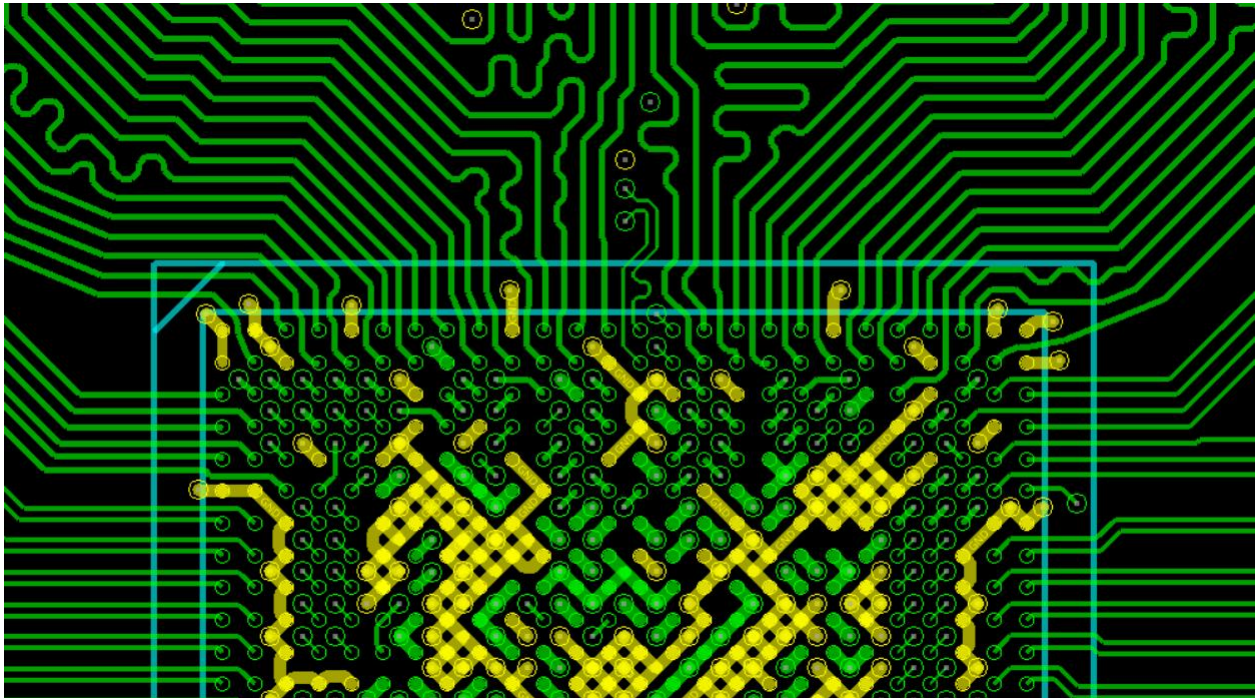
2.5.2 DDR – PCB Layout Recommended Design

For a 6-layer PCB, DDR signals are recommended on L1 and L4, with primary references to complete ground planes on L2 and L5. Incomplete GND planes significantly degrade signal quality. Maintain spacing and length requirements as shown in the table. Include pin_delay during routing.

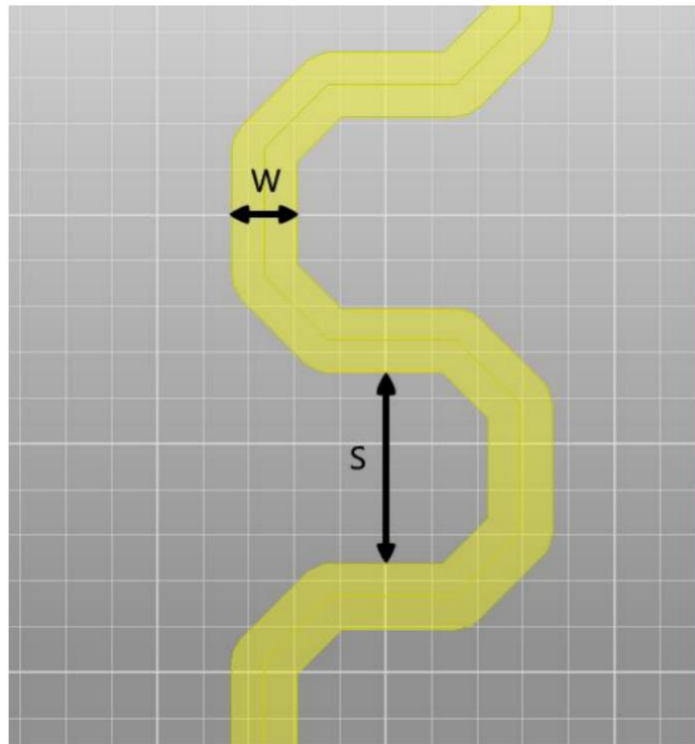
Parameter	Requirement
DDR single-ended impedance	$50\Omega \pm 10\%$
DDR differential pair impedance	$90\Omega \pm 10\%$
Spacing between different bytes	$\geq 3 \times \text{trace width}$
Spacing within a byte	$\geq 2 \times \text{trace width}$
Differential pair P/N length match	$\leq 5 \text{ mil}$
Same-byte group (CLK as target)	$\leq 50 \text{ mil}$

DDR design is challenging due to high interface speed. Use our DDR template and firmware, which are validated by simulation and testing. If designing your own PCB, follow these guidelines and simulate thoroughly before fabrication:

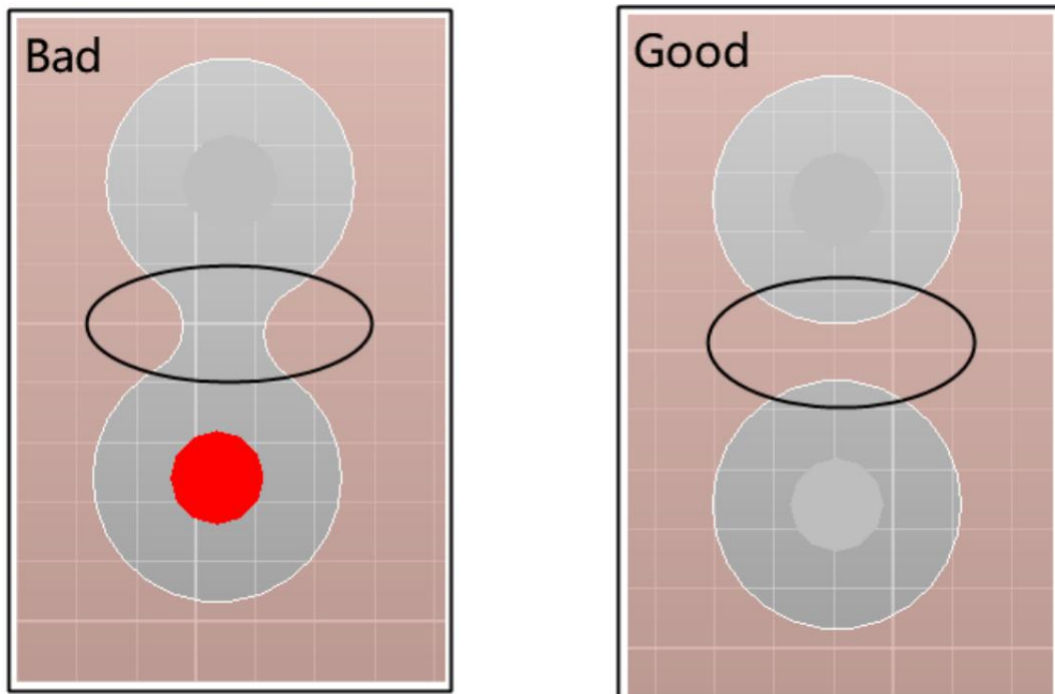
1. GND vias at CPU and DDR ends must follow the template; do not remove GND vias:



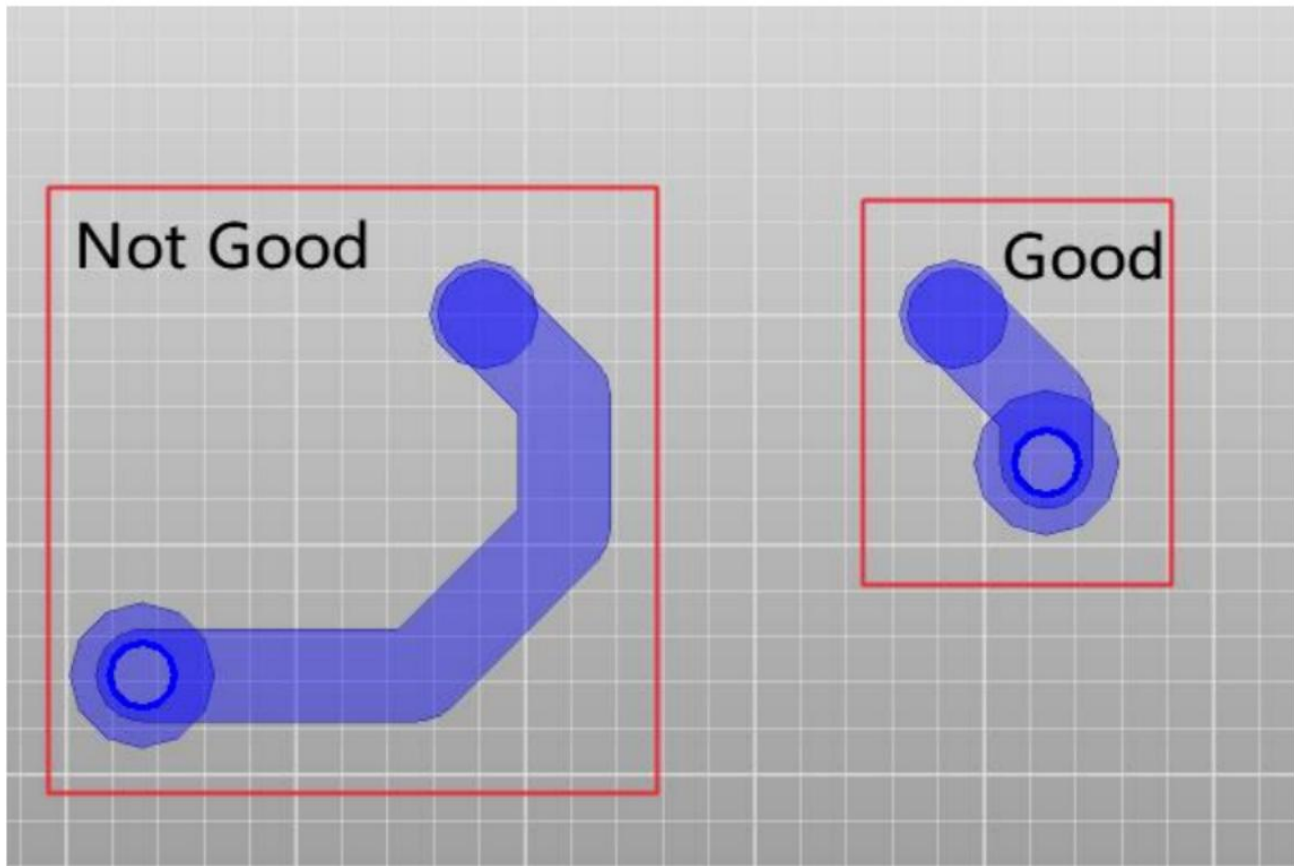
2. Routing crosstalk affects signal delay; for length-matched traces, maintain $S \geq 3W$:



3. DDR IC area: one GND via per pin; add more vias if space allows.
4. Adjust via positions and optimize plane splits to improve return paths:



5. Decoupling capacitors: each pad should have at least one via. For 0603/0805 caps, recommend two vias per pad, placed close to the pin to reduce loop inductance:



2.5.3 eMMC – PCB Layout Recommended Design

- Maintain CPU–eMMC spacing according to the reference board.
- If space is limited, minimize trace length between CPU and eMMC, ideally $\leq 1500\text{mil}$.
- For D0–D7, RE, WE, ensure length matching to CLK, within $\leq 100\text{mil}$.

2.6 Interface PCB Design

2.6.1 GMAC Signal PCB Design

Keep GMAC traces as short as possible and minimize layer transitions. Trace requirements:

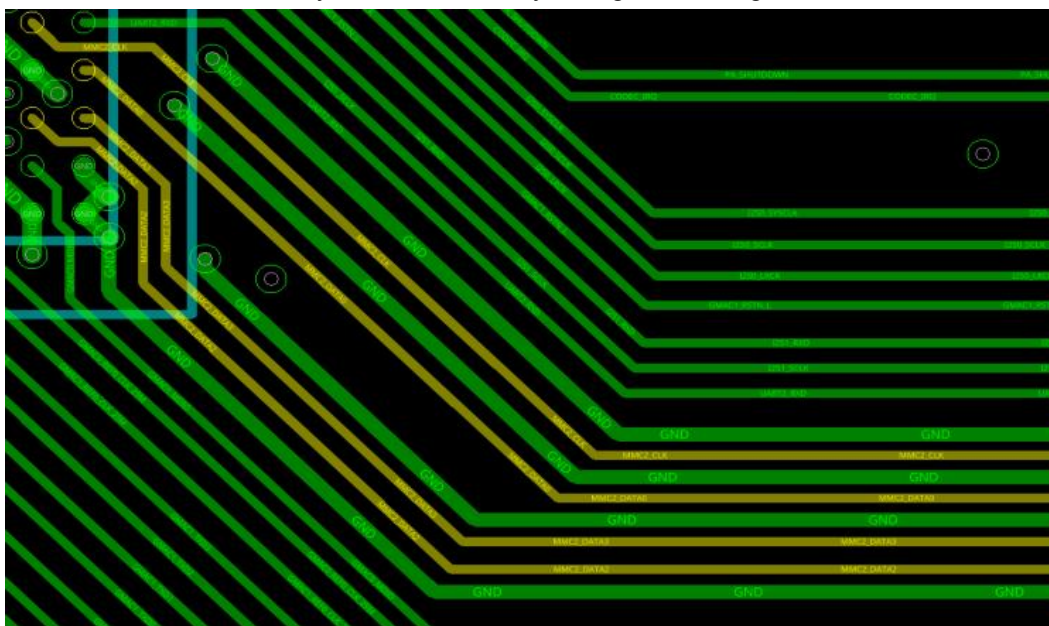
Parameter	Requirement
Trace impedance	Single-ended $50\Omega \pm 10\%$
Clock-to-data length matching	$< 100\text{ mil}$
Trace length	$< 4000\text{ mil}$
GMAC trace spacing	$3 \times \text{GMAC trace width}$

2.6.2 SDIO Signal PCB Design

- Avoid stubs on all SDIO traces; all traces must reference GND.
- Number of layer transitions (VIA) for each trace: ≤ 4 .
- Surround each SDIO trace with GND for signal stability.
- Preferred: CLK/CMD/DATA0-3 individually shielded. If space is limited:
 - ✧ CLK & CMD separately shielded
 - ✧ DATA0-DATA1 together, DATA2-DATA3 together

Parameter	Requirement
Trace impedance	Single-ended $50\Omega \pm 10\%$
Clock-to-data length matching	< 100 mil
Trace length	< 2500 mil
SDIO trace spacing	$3 \times$ SDIO trace width

Note: WiFi module SDIO traces must strictly follow the hardware design guide for PCB layout. After PCBA assembly, send the board to the factory for WiFi TX Delay tuning and testing.



2.6.3 USB2.0 Signal PCB Design

Parameter	Requirement
Trace impedance	Differential $90\Omega \pm 10\%$
Max P/N delay mismatch	≤ 5 mil
Trace length	< 5000 mil
Differential pair spacing	$\geq 3 \times$ USB trace width
Spacing to other signals	$\geq 3 \times$ USB trace width
Layer transitions (VIA)	≤ 3

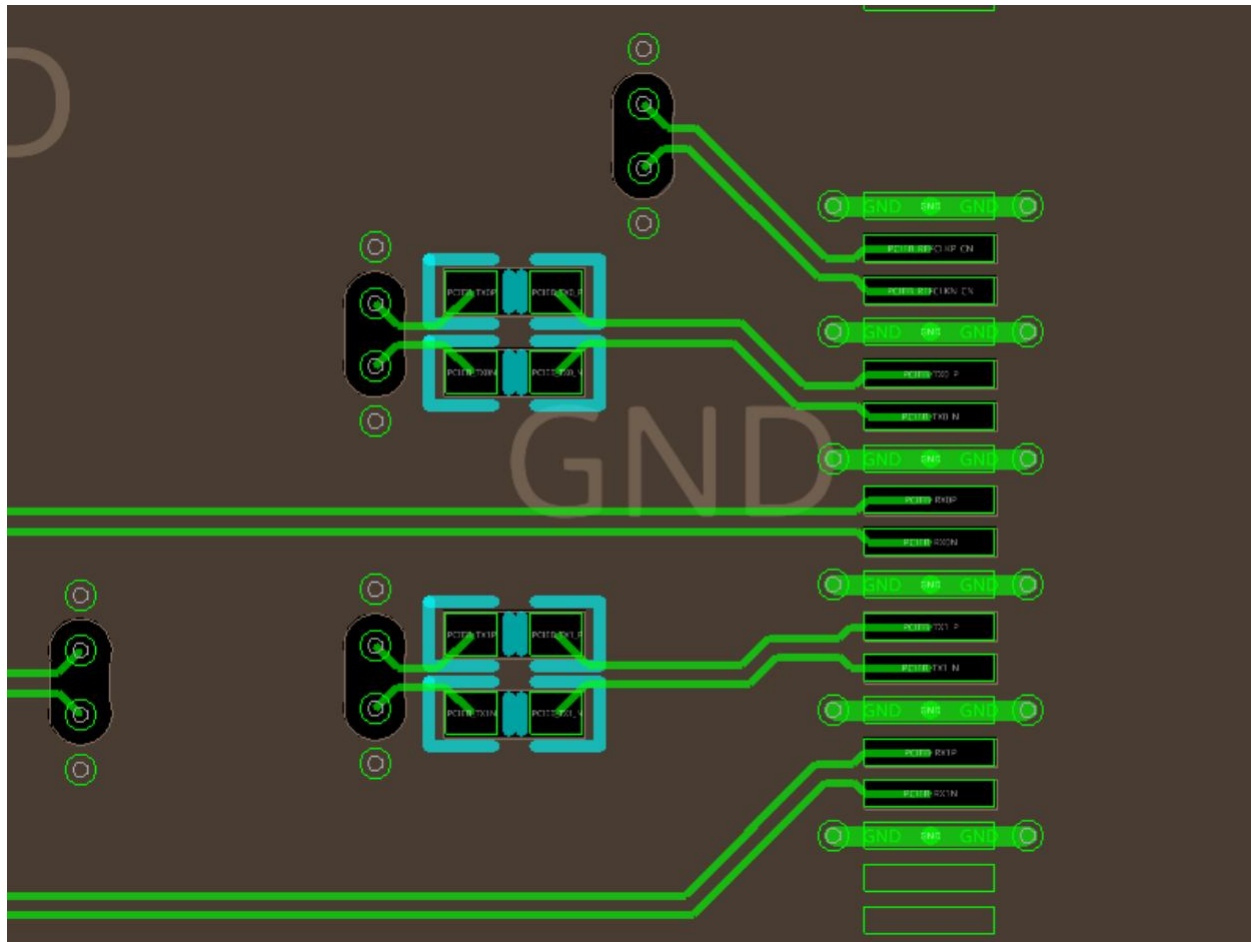
2.6.4 USB3.0 Signal PCB Design

Parameter	Requirement
Trace impedance	Differential $90\Omega \pm 10\%$
Max P/N delay mismatch	≤ 5 mil
Trace length	< 5000 mil
Differential pair spacing	$\geq 4 \times$ USB trace width
Spacing to other signals	$\geq 4 \times$ USB trace width
Layer transitions (VIA)	≤ 2

2.6.5 PCIE Signal PCB Design

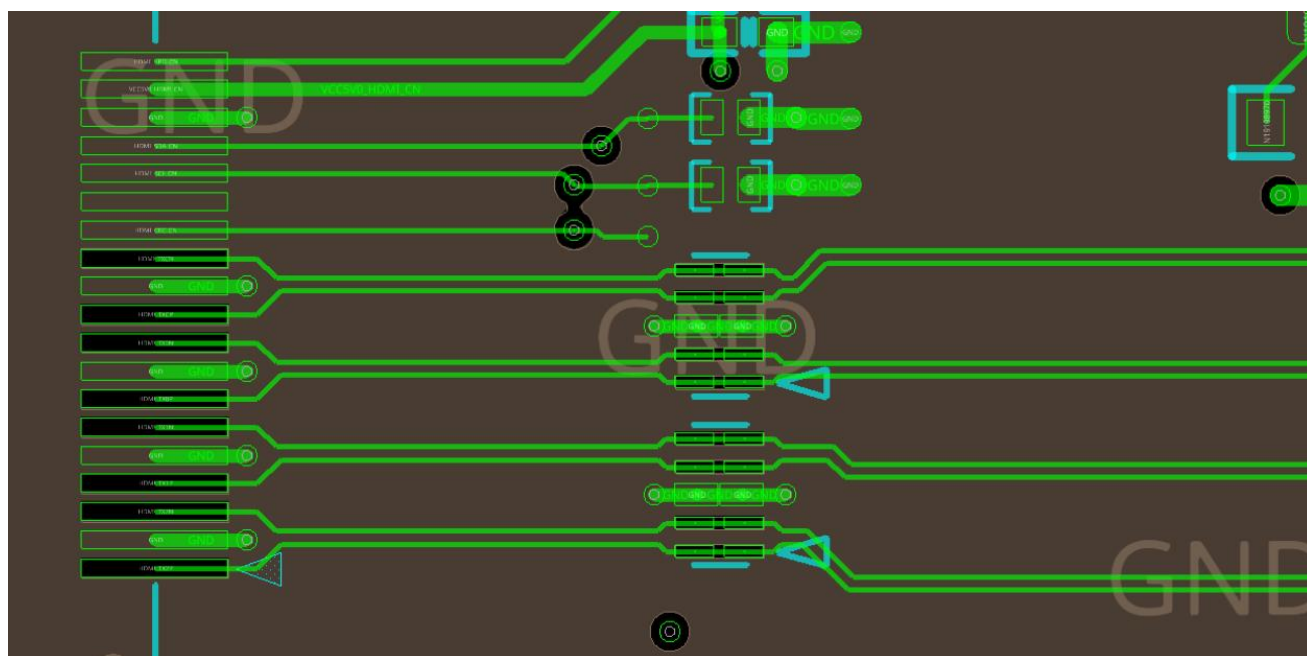
- Use anti-pad via clearance for PCIE pads.
- Avoid crossing reference planes; for GND-isolated pads, route ground traces both ways and place vias.

Parameter	Requirement
Trace impedance	Differential $90\Omega \pm 10\%$
Max P/N delay mismatch	≤ 5 mil
Trace length	< 4000 mil
Differential pair spacing	$\geq 5 \times$ PCIE trace width
Spacing to other signals	$\geq 5 \times$ PCIE trace width
Layer transitions (VIA)	≤ 2



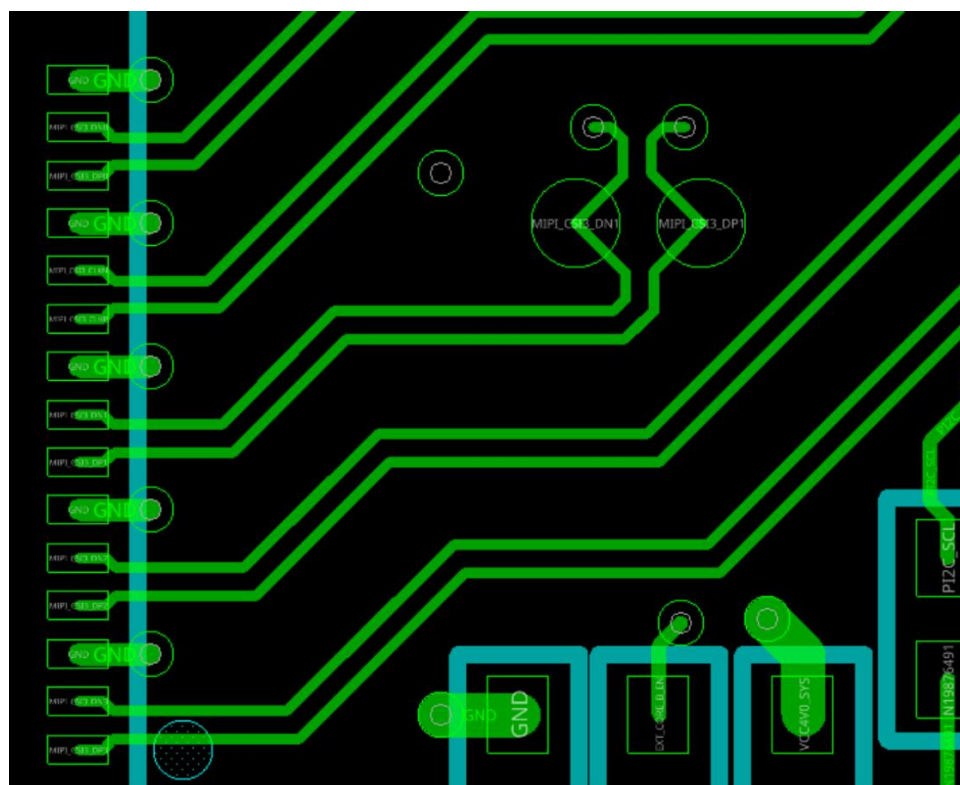
2.6.6 HDMI Signal PCB Design

Parameter	Requirement
Trace impedance	Differential $90\Omega \pm 10\%$
Max P/N delay mismatch	≤ 5 mil
Trace length	< 4000 mil
Differential pair spacing	$\geq 5 \times$ HDMI trace width
Spacing to other signals	$\geq 5 \times$ HDMI trace width
Layer transitions (VIA)	≤ 2



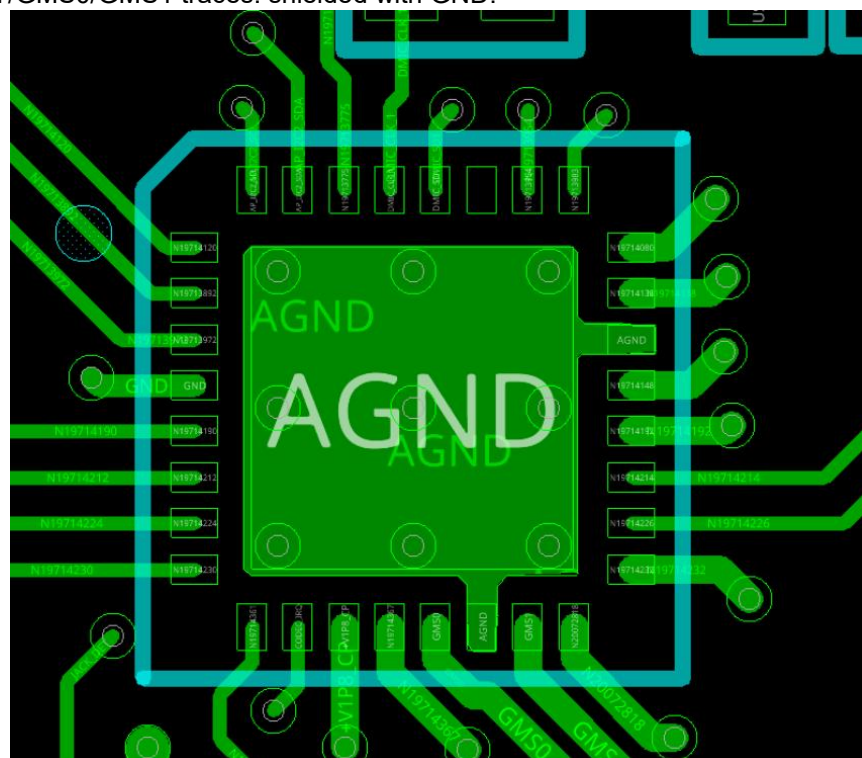
2.6.7 MIPI Signal PCB Design

Parameter	Requirement
Trace impedance	Differential $90\Omega \pm 10\%$
Max P/N delay mismatch	≤ 5 mil
Clock-to-data length matching	≤ 50 mil
Trace length	< 5000 mil
Differential pair spacing	$\geq 4 \times$ MIPI trace width (min $3\times$)
Spacing to other signals	$\geq 4 \times$ MIPI trace width (min $3\times$)
Layer transitions (VIA)	Recommended ≤ 2



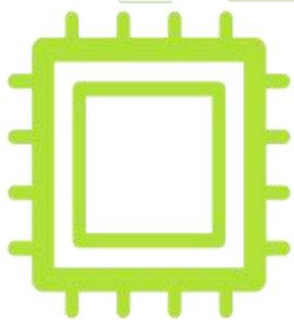
2.6.8 Audio PCB Design

1. Place GND vias evenly on thermal pads.
2. GMS0/GMS1 traces: 10mil width.
3. LOUT/ROUT/GMS0/GMS1 traces: shielded with GND.



Chapter 3

System-Level ESD Design

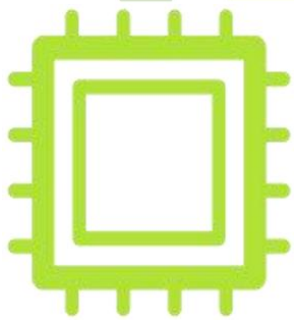


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- For the 24MHz system clock, use a 4-pin SMD crystal; connect the two GND pins fully to PCB ground to improve clock EMI immunity. Avoid routing signals under the crystal.
- During PCB layout, keep the small subsystem away from metal interfaces to enhance overall ESD performance.
- External connectors (AV I/O, USB, Ethernet, alarm ports) must have ESD protection devices.
- For floating-ground systems, avoid splitting ground under metal interfaces.
- PCB mounting holes should be metallized and connected to GND to ensure proper chassis grounding.
- For grounded systems, chassis must be connected to earth; connect protective and digital grounds at a single point, located away from small system circuits, preferably near the power connector.
- Connector housings should be metal and electrically connected to the chassis (e.g., HDMI, USB with screws; RJ45 with shielding tabs).

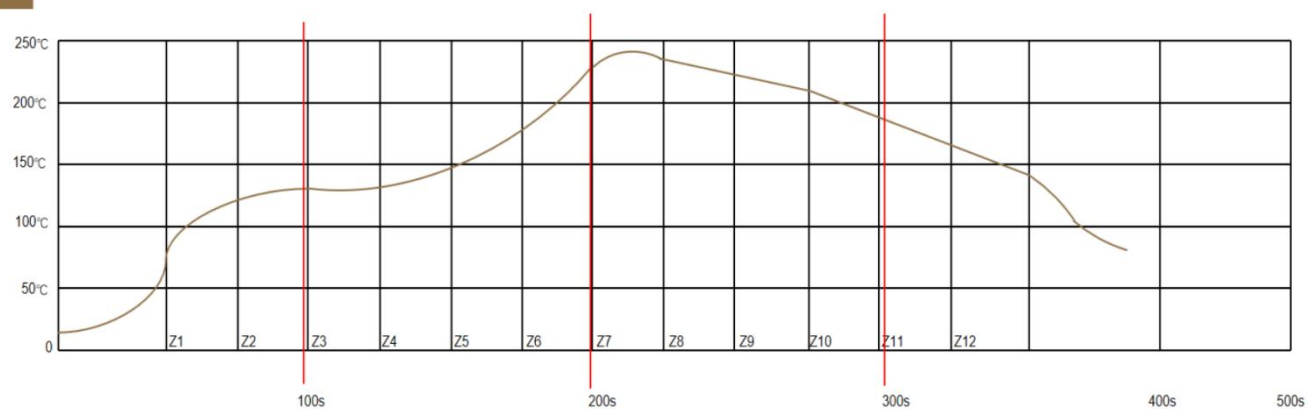
Chapter 4

Manufacturing Process

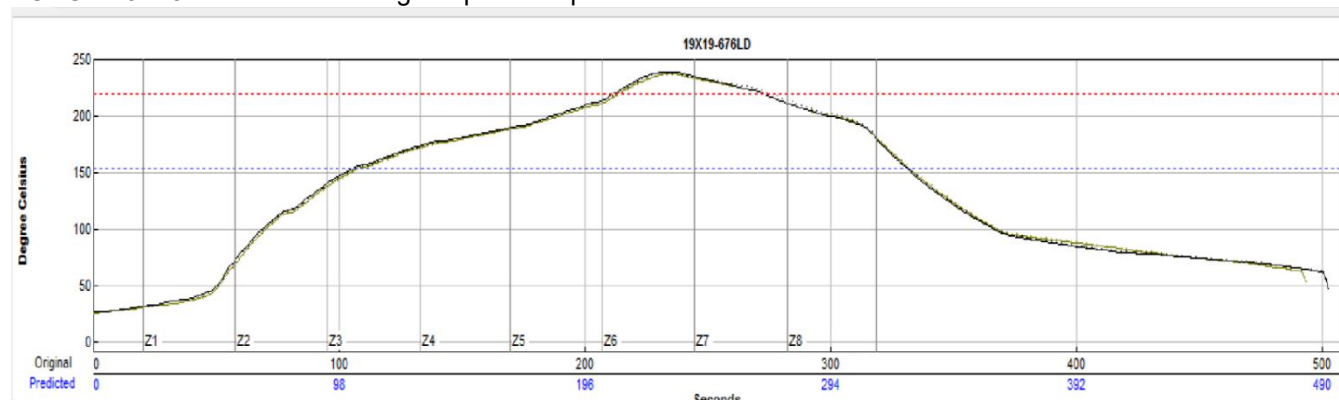


Key Stone® K1 Hardware Design Guide

FCCSP 17×17 – Reflow soldering temperature profile:



FCBGA 19×19 – Reflow soldering temperature profile:





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